08:30	**FPGAworld 2020 - Preliminary** **Registration Sep 17th, DTU (SCION), Building 372, Diplomvej 2800 Lyngby**
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09:00	**Conference opening** Professor Lars Dittmann, Technical University of Denmark and Lennart Lindh, FPGAworld
09:15-10:00	**Keynote** **Title:** Adaptable Domain-Specific Architecture (DSA) for AI inference **Keynote speaker:** Tero Rissa, Xilinx, Finland **Abstract:** Every day new AI models are being invented to achieve higher accuracy or lower hardware requirements. However, fixed AI accelerators such as GPUs and ASICs struggle to meet real-life performance due to increasing complexity in network layers, layer-to-layer dataflow and lower mixed precisions. In this talk, we will show various Domain Specific Architectures (DSA) to optimize CNN, LSTM, and MLP in different vectors such as throughput, latency, and hardware utilization. **CV:** Tero has more than 20 years of industrial experience of scaling new technologies from research and concept engineering into commercial products. He started working with artificial neural networks in 2009 and has since held senior positions in both engineering and management. Most recently he has been AI/ML HW Acceleration Research Group Leader at Nokia Bell Labs, Chief Architect of Machine Learning for Nokia Mobile Networks, the lead architect of OZO in Nokia Technologies and director of R&D at Microsoft. Tero holds MSc in CS/EE, Digital and Computer Systems from TUT Finland, and Ph.D. in Computing from Imperial College London UK. He is also an emeritus member of the Nokia CEO Technology Council and Bell Labs Distinguished Member of Technical Staff. **Session Chair:** Professor Lars Dittmann, Technical University of Denmark
10:00-10:30	**Coffee Break & Exhibition**
10:30-12:00 3*30 min	Industrial/Product Presentations Session Chair: Lennart FPGAworld **A: Significantly accelerating FPGA based development without compromising performance** **Speaker:** Weintraub, Gidel Inc, Israel **B: Microchip's next System On Chip device family: PolarFire SoC** **Speaker:** David Esselius, Microchip, Sweden one more free
12:00-13:00	**Lunch Break & Exhibition**

13:00-13:30	**FPGA events during the year that has gone and gossips** **Mike Dini talk,** Dini Group part of Synopsys, USA Session Chair: Rolf Sylvester-Hvid, Aktuel Elektronik, Denmark		
13:30-14:30 2*30 min	Industrial/Product Presentations Session Chair: Lennart FPGAworld Two free		
14:30-15:00	**Coffee Break & Exhibition**		
15:00-15:30	Industrial/Product Presentations Session Chair: Lennart FPGAworld One free		
15:30 -16:00	**Panel Session** **Title:** Does the FPGA education meet the industrial needs? **Moderator:** Rolf Sylvester-Hvid, Aktuel Elektronik, Denmark **Abstract:** The leading FPGA manufacturers have invested incredible resources in tools for FPGA development yet with limited success. Is the problem the education? Is the FPGA education today enough or must it be changed to meet the various challenges involved in developing and integrating FPGA based solutions? Does the gap between the needs in the industry and the results from education grows? Is it some areas education is missing today?		
16:00 -	**Go Home Drink in Exhibibition Hal**		
Sponsors, exhibitors and/or presenters Copenhagen and Stockholm	DTU, Technical University of Denmark ÅF, Sweden Aktuel Elektronik, Denmark Elektroniktidningen, Sweden Dini Group, USA Synective Labs, Sweden	Avnet Silica, Denmark Gidel, Israel Microchip, Sweden	Motion Control, Sweden AGSTU FPGA Education (Yrkeshögskola), Sweden
DTU	**Welcome to next FPGAworld Conference 2021** **Stockholm 14 September and Copenhagen 16 September**		FPGA™ world

More information

Keynote Speakers Copenhagen

Keynote speaker: Tero Rissa, Xilinx, Finland

Title: Adaptable Domain-Specific Architecture (DSA) for AI inference

Abstract: Every day new AI models are being invented to achieve higher accuracy or lower hardware requirements. However, fixed AI accelerators such as GPUs and ASICs struggle to meet real-life performance due to increasing complexity in network layers, layer-to-layer dataflow and lower mixed precisions. In this talk, we will show various Domain Specific Architectures (DSA) to optimize CNN, LSTM, and MLP in different vectors such as throughput, latency, and hardware utilization.

About the presenter: Tero has more than 20 years of industrial experience of scaling new technologies from research and concept engineering into commercial products. He started working with artificial neural networks in 2009 and has since held senior positions in both engineering and management. Most recently he has been AI/ML HW Acceleration Research Group Leader at Nokia Bell Labs, Chief Architect of Machine Learning for Nokia Mobile Networks, the lead architect of OZO in Nokia Technologies and director of R&D at Microsoft. Tero holds MSc in CS/EE, Digital and Computer Systems from TUT Finland, and Ph.D. in Computing from Imperial College London UK. He is also an emeritus member of the Nokia CEO Technology Council and Bell Labs Distinguished Member of Technical Staff.

Industrial Presentations

Title: Significantly accelerating FPGA based development without compromising performance

Abstract : FPGA technology offers significant advantages in diverse applications. However, the dispersion of FPGA technology has been limited due to the various challenges involved in developing and integrating FPGA based solutions. While FPGA is reconfigurable by nature, it requires the expertise of FPGA designers and is not within the scope of most software engineers, thus limiting significantly the number of qualified personnel who can develop on FPGA. The leading FPGA manufacturers have invested tremendous resources in tools for FPGA development yet with limited success. Moreover, developing and integrating a custom solution requires the cooperation of a board designer, an FPGA designer, an algorithm developer and a software engineer. As such, the complexity of developing on FPGA incorporates substantial obstacles that deter many companies from accessing the tremendous potential offered by FPGA.

In his talk, Mr. Reuven Weintraub, Founder and CTO of Gidel Inc., will elaborate on advanced tools and methodology for simplifying and significantly accelerating development on FPGA without compromising the final system's performance. Based on these tools key development bottlenecks are overcome enabling to reduce development time by 50% and beyond. Mr. Weintraub will expand on the possibility for replacing time consuming manual HDL designing with tools that automatically map the FPGA platform resources to the application needs thus reducing development time while enhancing system reliability and simplifying the system integration. The talk will address the fundamental challenges involved in FPGA development and present an innovative approach to developing and harnessing FPGA power to achieve versatile implementations while reducing development time and optimizing performance.

About the presenter: Mr. Weintraub, Gidel's founder and CTO, is a long-standing system architect and algorithms guru for FPGA based systems. He has led many innovations, some considered as mission

impossible, such as retrieving lost data from JPEG compression. Prior to founding Gidel Ltd in 1993, Mr. Weintraub served 10 years in Medical Imaging companies in both technical and management positions. Mr. Weintraub holds an MSc. in Electronic Engineering and a BSc. in Computer Engineering from the Technion Institute of Technology Haifa Israel.

Product Presentations

Title: Microchip's next System On Chip device family: PolarFire SoC

Speaker: David Esselius, Microchip, Sweden
Abstract: A presentation of Microchips next System On Chip device family PolarFire SoC that builds upon the flash-based FPGA family PolarFire and also integrates a powerful RISC-V processor core cluster within the same chip.

The Processor cluster is organized with one monitor core and 4 application cores capable of running operating systems like Linux on all the cores or running a mixture of operating systems. The processor subsystem provides a variety of standard IO interconnection as well as the first stage and secondary stage cache memory for the cores.

The heritage of low power, obscene of configuration memory upsets, and security functions housed by the FPGA part of the device makes it suitable for various demanding to compute-intensive applications.

About the presenter: David works as Embedded Solutions Engineer, specialized in Microchip FPGA devices in the Nordic countries, since 2019. Previously he worked as an FPGA designer for Saab Avionics and developed safety-critical applications for airborne equipment since 2005 and as general hardware designer since 1994.

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