


08:30	<p align="center"><b>FPGAworld 2019</b>  <b>Registration: Stockholm, Sep 17th, Frösundaleden 2A, 169 70 Solna, SWEDEN</b></p>		
<p align="center"><b>Thank you Sponsors!</b></p> 			
09:00	<p align="center"><b>Conference Opening</b>  Björn Eriksson, ÅF and Lennart Lindh, FPGAworld  Room: Devoted 09</p>		
09:15-10:00	<p align="center"><b>Keynote</b>  <b>Where do FPGA's outperform GPU's</b>  <b>Keynote speaker:</b> David Thomas, Intel PSG  Room: Devoted 09</p> <p><b>Abstract:</b> David Thomas will talk about the big picture and market segments where FPGA based acceleration plays at its best! Is all about TCO (Total Cost of Ownership), Performance/Watt ratio's from the Edge to the Datacenter (and back). The latency, power efficiency and ability to handle various workloads will be the critical parameters defining the HW choices of our Users/customers. In addition to having an agnostic, high level SW tool. (<a href="#">more info</a>)</p> <p align="right">Session Chair: Lennart Lindh, FPGAworld</p>		
10:00-10:30	<p align="center"><b>Coffee Break &amp; Exhibition</b></p> 		
10:30-12:00 3*30 min	<p align="center"><b>Industrial/Product Track</b>  Session Chair: Lennart Lindh,  FPGAworld  Room: Devoted 09</p>	<p align="center"><b>Product Track</b>  Session Chair:  Jesper Dahlbäck, FPGAworld  Room: Devoted 04</p>	<p align="center"><b>Product Track</b>  Session Chair:  Magnus Karlsson,  Innowicom System Solutions AB  Room: Brave 05</p>
	<p><b>A: VHDL-2019 - What is important and Why</b>  Jim Lewis, SynthWorks Design Inc and chair of the IEEE VHDL Working Group, USA (<a href="#">more info</a>)</p> <p><b>C: Identifying &amp; Correcting difficult to find RTL problems earlier</b>  Adam Taylor, Blue Pearl Software</p> <p><b>C: OpenVino – An introduction to Intel's OpenVino Toolkit</b>  Nikolay Rognlien, Arrow Norway AS, Norway</p>	<p><b>C: Adopting Model-Based Design for FPGA, ASIC, and SoC Development</b>  Daniel Aronsson, MathWorks, USA</p> <p><b>C: Addressing FPGA HLS (High-level Synthesis) challenges for heterogenous computing at the edge</b>  Juan Eusse, Silexica, Germany</p> <p><b>C: Linux, Yocto and FPGAs</b>  Anders Törnqvist, Codiax, Sweden (<a href="#">more info</a>)</p>	<p><b>C: Silicon Labs Clock Solutions</b>  Mike Ireland, Silicon Labs, USA</p> <p><b>C: Low Power AI and Machine Learning Ecosystem for products at the edge</b>  Matt Holdsworth, Lattice Semiconductor, USA (<a href="#">more info</a>)</p> <p><b>C: Vincent CDC Platform - A complete solution for Multiple Clock Domain FPGA design</b>  Reuven Dobkin, vSync Circuits, Israel (<a href="#">more info</a>)</p>
12:00-13:00	<p align="center"><b>Lunch Break &amp; Exhibition and Poster Session</b></p> 		
13:00-13:30	<p align="center"><b>Mike Dini talk, Dini Group, USA</b>  <b>FPGA events during the year that has gone and gossips</b>  Session Chair: Lennart, Room: Devoted 09</p>		
13:30-13:45	<p align="center"><b>Break &amp; Exhibition</b></p>		

	<b>Industrial/Product Track</b> Session Chair: Magnus Karlsson, Innowicom System Solutions AB Room: Devoted 09	<b>Industrial Track</b> Session Chair: Lennart Lindh, FPGAworld Room: Devoted 04	<b>Product Track</b> Session Chair: Kim Petersen, HDC AB Room: Brave 05
13:45-14:45 2*30 min	<p><b>A: How to accelerate the development of your embedded visions system?</b> Andrea Leopardi, BitSim, Sweden (<a href="#">more info</a>)</p> <p><b>C: Everything you need to accelerate innovation</b> Yehoshua Shoshan, Innofour</p>	<p><b>A: Getting Started with OSVVM, VHDL's #1 FPGA Verification Library</b> Jim Lewis, SynthWorks Design Inc and chair of the IEEE VHDL Working Group, USA (<a href="#">more info</a>)</p> <p><b>A: Introduction to FPGA VHDL Verification – using the world-wide exploding UVVM</b> Espen Tallaksen, Bitvis and CGI, Norway (<a href="#">more info</a>)</p>	<p><b>C: Functional Safety for FPGAs</b> Stefan Bauer, Mentor Booked</p> <p><b>C: FPGA-based security solutions for IoT and Industry 4.0</b> Matti Tommiska, Xiphera Oy (<a href="#">more info</a>)</p>

14:45-15:15 **Coffee Break & Exhibition** 

15:15-16:00	<p align="center"><b>Keynote</b> <b>Build and Debug Highly Reliably FPGA-based Designs</b> <b>Keynote speaker:</b> Madhav Chikodikar, Director of R&amp;D, Synopsys, Inc.</p>  <p><b>Abstract:</b> In today's complex FPGA designs there is a need to integrate an ability to most effectively and economically deploy SEU mitigation and error monitoring circuitry in their FPGA-based systems targeting high radiation environments. In the overall design of a system, there is an opportunity to take advantage of triple modular redundancy (TMR) for creating an error detection and mitigation scheme. Important considerations include area and power increase, which affect system cost and can in some cases increase the probability of an SEU and the overall design performance challenges when applying the techniques. This presentation discusses the debug of these mitigation techniques available for different types of FPGAs. Also, the talk is about how complete some simple testing of voter logic and triplicates within the error detection and correction schemes. The combined capability of debug and fault injection allow developers to easily see each triplication and voter to verify and monitor whether the SEU mitigation techniques are working as expected. The last part is a discussion of future development to build highly reliably FPGA- based design.</p> <p align="center">Session Chair: Lennart Lindh, Room: Devoted 09</p>
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16:00- **Go Home Drink in the Exhibition hall** 

Exhibitors and Product Presenters Copenhagen and Stockholm	<p>DTU, Technical University of Denmark ÅF, Sweden Aktuel Elektronik, Denmark Elektroniktidningen, Sweden Dini Group, USA Intel PSG, USA Mentor – A Siemens Business XILINX, USA SILEXICA, Germany PyramidTech, USA</p>	<p>GOWIN, China Lattice, USA Avnet Silica, Denmark Avnet Silica, Sweden Synopsys, USA BitSim, Sweden Blue Pearl Software, USA Xiphera, Finland SynthWorks, USA Bitvis and CGI, Norway VSYNC Circuits, Israel</p>	<p>Arrow, Europe Silicon Labs, Finland InnoFour, Netherlands Synective Labs, Sweden Blue Pearl Software Inc, USA MathWorks, USA CodiAx, Sweden Motion Control, Sweden AGSTU FPGA Education (Yrkeshögskola), Sweden</p>
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Welcome to next FPGAworld Conference 2020  
Stockholm 15 September and Copenhagen 17 September



## More information

### Two posters:

#### Boothng via CAN for GR716 microcontroller (student project)

**Abstract:** Presentation is based on internship at Cobham Gaisler. Cobham Gaisler develops IP cores for fault-tolerant and radiation-hardened electronics used in aerospace. Technical task was to develop a protocol that can be used for directly accessing memory addresses on target devices (GR716 Microcontroller) using CAN bus. GR716 is booted with CAN routine stored on SPI memory and executes commands that are encoded from received CAN frames from master device.

Event: Stockholm

**Presenter:** Aleksejs Sencenko, AGSTU education

#### Implementation of Measurement System Heimdall for UAV Detection (student project)

Heimdall is a system designed to develop algorithms for drone detection. The goal of Heimdall is to be able to pinpoint where a drone is in azimuth and elevation (2D) from a fixed position based on the incoming sound. Heimdall is designed to be expanded until it has a coverage of 360 degrees in azimuth angle while at the same time having enough computing power to process all the data in real time. To keep the system relatively simple to program, but still have the capacity for extended usage, the hardware used is a combination of an Arm-processor and a FPGA (Xilinx Zynq-7000).

**Presenter:** David Hillerström, AGSTU education

### Presenters:

#### VHDL-2019 - What is important and Why

**Abstract:** VHDL-2019 adds numerous features that are targeted at verification improvement. These include: interfaces, protected type improvements, an API for Assert and PSL, and conditional compilation. Interfaces allow models to handle an interface connectivity abstractly. Protected types are used to create verification data structures, such as scoreboard, coverage modeling, ... The improvements provide the next step in modeling capability. The API for Assert and PSL allows tests to get a count of errors from these sources. Jim is chair of the IEEE VHDL Working Group.

**Presenter:** Stockholm, Copenhagen

From: Jim Lewis, SynthWorks Design Inc, USA

#### Identifying & Correcting difficult to find RTL problems earlier

**Abstract:** All engineers know the earlier we identify an issue in our design, the easier and less costly it is to correct. The worst issues are intermittent and manifest late in test or worse in the field. These late issues lead to long hours and stress in the engineering team. This session will explore common design issues which can cause these hard to find late issues, how we can address them along with outlining how they can be identified easier using Blue Pearl's Visual Verification Suite

**Presenter:** Adam Taylor, Blue Pearl Software, USA

Company website: <https://www.bluepearlsoftware.com/>

#### OpenVino – An introduction to Intel's OpenVino Toolkit

**Abstract:** Intel is investing heavily in the Computer Vision solutions with both hardware and software tools to enable customers to be efficient and competitive.

This session gives you an introduction to how Intel's distribution of "OpenVino toolkit" may help you convert a trained model from high level tools like TensorFlow and Caffe, to be inferenced on various hardware architectures, including FPGAs. This is applicable both for servers as well as embedded applications.

Presenter: Nikolay Rognlien, Arrow Norway AS, Norway

#### Adopting Model-Based Design for FPGA, ASIC, and SoC Development

**Abstract:** In this presentation we talk about how to adopt Model-Based Design for chip design.

We start by defining the problem that this approach solves.

Then we describe how to adopt this approach incrementally in ways that help workflows the most.

Finally we will show results from a key customer.

Event: Stockholm

**Presenter:** Daniel Aronsson, MathWorks, USA

Company website: [www.mathworks.com](http://www.mathworks.com)

### Addressing FPGA HLS (High-level Synthesis) challenges for heterogeneous computing at the edge

**Abstract:** In this presentation we examine how SLX FPGA is used to take a MATLAB Embedded Coder™ generated C/C++ algorithm, in this case a Kalman filter, and optimize the C/C++ code for HLS. In this example, SLX FPGA provides more than 62x improvement in performance after auto-insertion of HLS pragmas when compared to the solution created by the HLS compiler for the original code, which had no pragmas inserted.

Event: Stockholm ( Reserve Copenhagen)

**Presenter:** Juan Eusse, Silexica, Germany

Company website: [www.silexica.com](http://www.silexica.com)

### Linux, Yocto and FPGAs

**Abstract:** Integrating Linux and Yocto builds into different SoCs requires many things to manage, both technical and practical. Most of this is also applicable when integrating into FPGAs containing CPU cores that can run Linux.

Event: Stockholm

**Presenter:** Anders Törnqvist, [www.codiax.se](http://www.codiax.se)

### Silicon Labs Clock Solutions

**Abstract:** Silicon Labs offers the industry's broadest portfolio of crystal oscillator, clock generator, clock buffer, and jitter attenuator products and PCI Express (PCIe) clock generators and PCI Express buffers. Silicon Labs' patented technology combines best-in-class frequency flexibility with the lowest jitter in the industry, delivering quick-turn, customized solutions that simplify board design, eliminate discrete components, and maximize system performance.

Event: Stockholm

**Presenter:** Mike Ireland, [www.silabs.com](http://www.silabs.com)

### Low Power AI and Machine Learning Ecosystem for products at the edge

**Abstract:** With faster decisions, privacy concerns and network bandwidth considerations, AI-based designers are increasingly looking to move inferencing functions out of the cloud and to the edge. Lattice small low power FPGAs and Lattice sensAI stack simplifies AI solutions for smart IoT devices. Full-featured Lattice sensAI stack includes modular hardware platforms, neural network IP cores, software tools, reference designs, and partner design services. These Flexible inferencing solutions are optimized for <1 mW-1 W, on FPGA packages from 5.5 mm<sup>2</sup>.

Event: Stockholm

**Presenter:** Matt Holdsworth, [www.latticesemi.com](http://www.latticesemi.com)

### Vincent CDC Platform - A complete solution for Multiple Clock Domain FPGA design

**Abstract:** vSync Circuits Vincent CDC Platform consists of a number of EDA tools and IP libraries, enabling reliable integration and verification of multiple-clock domain designs. In addition to providing the static CDC analysis and Lint, Vincent CDC platform supports different FPGA and ASIC design flows, including simulations at RTL and gate-level. The platform identifies CDC bugs and creates auto-customized RTL solutions. The tools enable fast design CDC and Lint analyses, design reliability assessment (MTBF) and an automated bug fixing.

**Presenter:** Reuven Dobkin, <[reuven@vsyncc.com](mailto:reuven@vsyncc.com)>

Event: Stockholm

### ---- afternoon program -----

#### How to accelerate the development of your embedded vision system?

**Abstract:** It is a huge task to cover everything from data collection, from for example RGB- or IR-sensors, to data analysis and, perhaps, to make decisions depending on results. BitSim has developed a platform integrating both sequential (CPU) and parallel (FPGA) processing to implement all these steps more straightforward and faster. From

embedded vision to Deep Learning, and from VHDL to Python, the entire stack is integrated into a single application making your development more agile.

Event: Stockholm, Copenhagen

**Presenter:** Andrea Leopardi, BitSim AB, Sweden

Comapany website: [www.bitsim.com](http://www.bitsim.com)

### Everything you need to accelerate innovation

**Abstract:** Embedded software is in virtually all the products we come in contact with everyday.

As a result the use of embedded software is quickly infringing on hardware's dominance in the product development process. This presentation will cover the challenges in today's embedded software development and how we can help organizations with a unified solution that divers project transparency through real-time aggregated management information.

Event: Stockholm, Copenhagen

**Presenter:** Yehoshua Shoshan, InnoFour

Comapany website: [www.innofour.com](http://www.innofour.com)

### Getting Started with OSVVM, VHDL's #1 FPGA Verification Library

**Abstract:** The 2018 Wilson Research Group ASIC and FPGA Functional Verification Study revealed that Open Source VHDL Verification Methodology (OSVVM) is the #1 VHDL FPGA verification library in the world.

This getting started guide to OSVVM covers how to write transaction-based tests, message filtering, error checkers, functional coverage, constrained random tests, scoreboards, synchronization methods, and testbench utilities OSVVM's simple, readable, and powerful methodology provides a complete solution for FPGA or ASIC verification.

Event: Stockholm, Copenhagen

**Presenter:** Jim Lewis, SynthWorks Design Inc, USA

### Introduction to FPGA VHDL Verification – using the world-wide exploding UVVM

**Abstract:** There is a huge efficiency and quality potential in making good and well-structured testbenches. This applies to most developers and most companies. Improvement here is actually easy and does not require any investment at all. In fact – if you do this right – you will save a lot of time and improve quality already in your first project. The examples used are from the open source Universal VHDL Verification Methodology, but they show best practices for modern VHDL verification. UVVM has exploded over the last two years from 0 to 10% world-wide and increasing faster than ever. UVVM is recommended by Doulos for TB architecture, and we are cooperating with ESA to extend the functionality even further.

This presentation will show you the basics of making good testbenches, give you a fast introduction to UVVM Utility Library, BFM's and VVC's, - and show you step-by-step how to get started in only 4 minutes.

Event: Stockholm

**Presenter:** Espen Tallaksen, Bitvis and CGI, Norway

### Functional Safety for FPGAs

**Abstract:** Everybody is talking about and many companies are jumping on the functional safety train. The latest industry study from the Wilson Research Group shows, that almost 2/3 of today's European FPGA design projects are used within a safety application, i.e. autonomous driving or airplanes. Such safety applications require a high quality and a high reliability of the FPGAs. But the truth is, that more than 70% of these FPGA designs still have non-trivial bugs which escape to production. Functional Safety is driving down risk of Electrical and Electronics malfunctioning due to failures. Standards like ISO 26262 or IES 61508 focus on two areas of faults: Systematic Faults and Random Faults. In this presentation Stefan Bauer, one of Mentor's verification experts, will give an introduction to the ISO 26262 standard and how Mentor's overall functional safety flow can help to verify Systematic Faults and Random HW Faults.

Event: Stockholm, Copenhagen

**Presenter:** Stefan Bauer

Comapany website: <https://www.mentor.com/>

## FPGA-based security solutions for IoT and Industry 4.0

**Abstract:** This presentation discusses the benefits of FPGA-based security solutions and compares them to the software-based approach for addressing the challenges of Industry 4.0 and IoT. After a short introduction to cryptography, the main content of the presentation is an example of an FPGA-based communications endpoint implementation.

Event: Stockholm

Presenter: Matti Tommiska, Xiphera Oy, Finland

Company website: <http://www.xiphera.com>



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