







08:30	<p align="center">FPGAworld 2018 - Tutorial Registration; Stockholm, Sep 18th, Frösundaleden 2A, 169 70 Solna, SWEDEN</p>
<p align="center">Sponsors:     </p>	
10:00-10:30	<p align="center">Coffee Break & Exhibition (free to sponsor)</p>
10:30-12:00	<p>Contribution D – Tutorials (1,5 hours)</p> <p><u>VUnit 3 - Develop Code with Confidence and Speed</u></p> <p>Time: 10:30 – 12:00 Room: Älgen Two compulsory registrations: send e-mail to tutorial@synective.se and registration on the FPGAworld (max 12 persons).</p> <p>VUnit (vunit.github.io) is an open source testing framework for VHDL and SystemVerilog founded in 2014 by Lars Asplund from Synective Labs and Olof Kraigher from Veoneer. It features the functionality needed to realize continuous and fully automated testing of your HDL code.</p> <p>VUnit doesn't replace but rather complements traditional testing methodologies by reducing test overhead. Tests can be run earlier and more frequent and bugs can be found before they become costly. VUnit improves the speed of development by supporting incremental compilation and by enabling large test benches to be split up into smaller tests executed in parallel. It increases the quality of projects by enabling large regression suites to be run on a continuous integration server.</p> <p>VUnit does not impose any specific verification methodology on its users. The benefits of VUnit can be enjoyed when writing tests first or last, when writing long-running top-level tests or short and fast unit tests, when using directed or constrained random testing. VUnit also includes libraries for supporting common verification tasks.</p> <p>VUnit is used by both FPGA and ASIC teams, from US to Japan, when developing everything from high-volume products like automotive vision to niche military systems, by tool providers, in research and education.</p> <p>In this tutorial you will learn how you can get started by adopting your existing test benches in a few small steps. We will explore the everyday tasks performed by a VUnit user: adding test cases, running full or partial test suites, multi-core test execution, debugging failing test cases etc. You will also get acquainted with the support libraries provided by VUnit, for example logging, checking, advanced test bench communication, and bus functional models.</p>
12:00-13:00	<p align="center">Lunch Break & Exhibition Sponsor </p>
13:30-13:45	<p align="center">Break & Exhibition</p>

Contribution D – Tutorials (1 hours)

Flyover Cabling Solutions for High Performance Interconnect for FPGAs

Time: 13:45-14:45

Room: Älgen

Two compulsory registrations: send e-mail to Kevin.Burt@samtec.com and registration on the FPGAworld (max 12 persons).

13:45-14:45

As FPGA speeds increase to 56/112 Gbps PAM4, and the number of transceivers increase, so do the system design challenges. Signal integrity, thermal and packaging considerations place extreme constraints on the entire path out of the FPGA.

Traditional PCB routings are limited by the material resulting in shorter traces or more expensive exotic materials and layout challenges getting all the 56/112 G signals routed. As a result, the Interconnect Industry has created flyover cable solutions to enable these high bandwidth, high density links. These flyover solutions enable improved Signal integrity, low system power, and high performance, high density FPGA connections by taking the high speed signals off board and into low loss cables.

In this tutorial, you will learn the challenges of using traditional PCB layout techniques as well as the advantages of copper and optical cables as well as the system advantages that they enable.”

Welcome to next FPGAworld Conference 2019

Preliminary: Stockholm 17 September and Copenhagen 19 September

Please marketing the event