FPGA World 2018 - Stockholm & Copenhagen

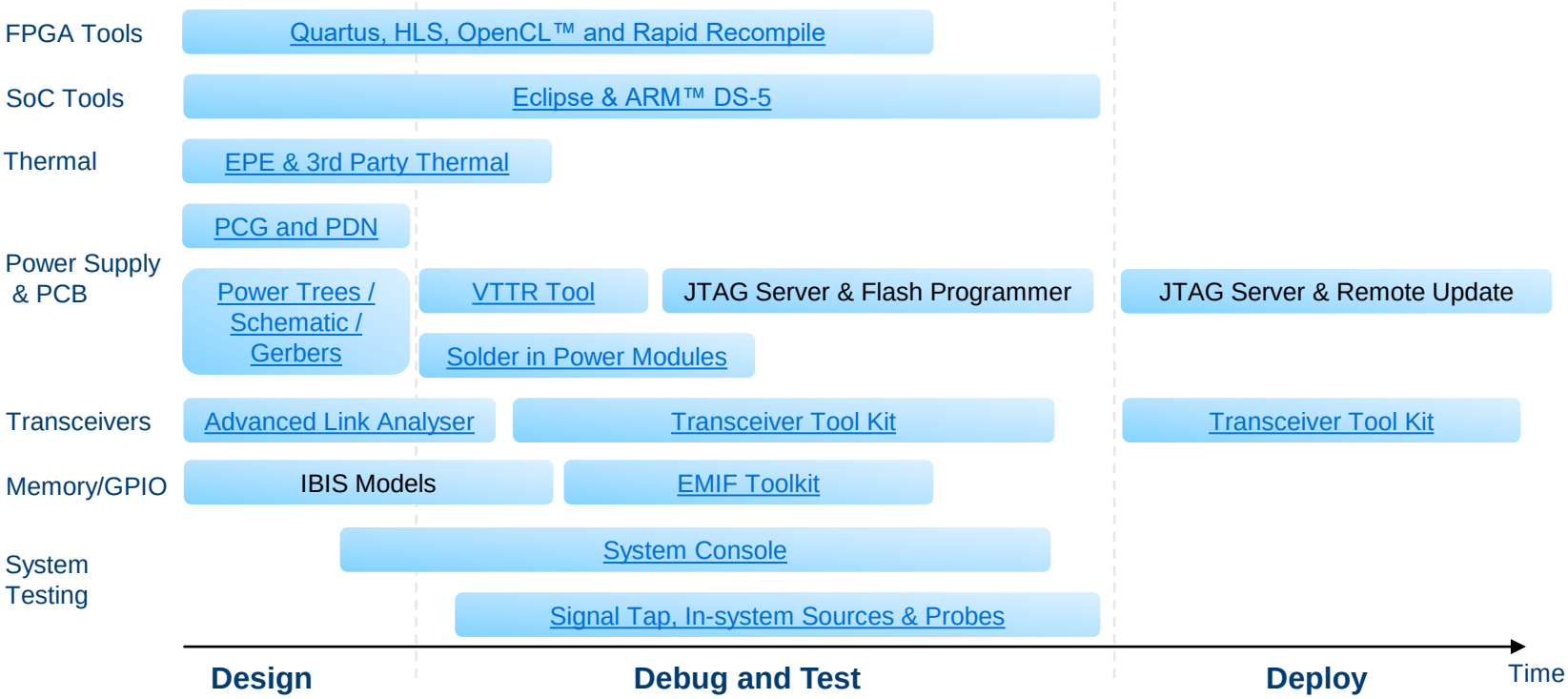
Debug Tools and Methods

Nikolay Rognlien – Arrow FPGA Market Developmet Engineer

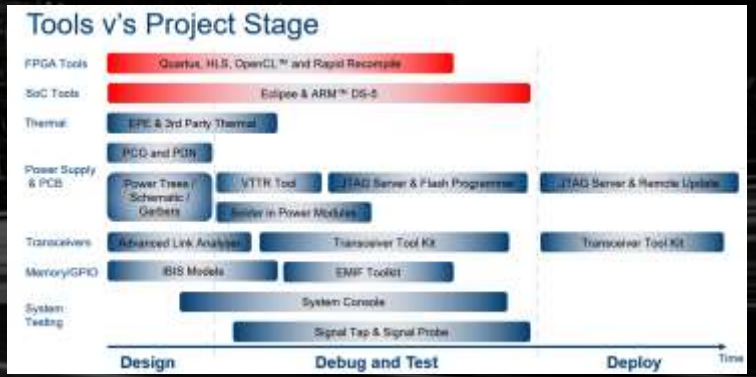
Five Years Out

Tools v's Project Stage

Hyperlinked to Slides in this Presentation



Quartus Prime and ARM Tools for Debug



Quartus Tips from the Experts

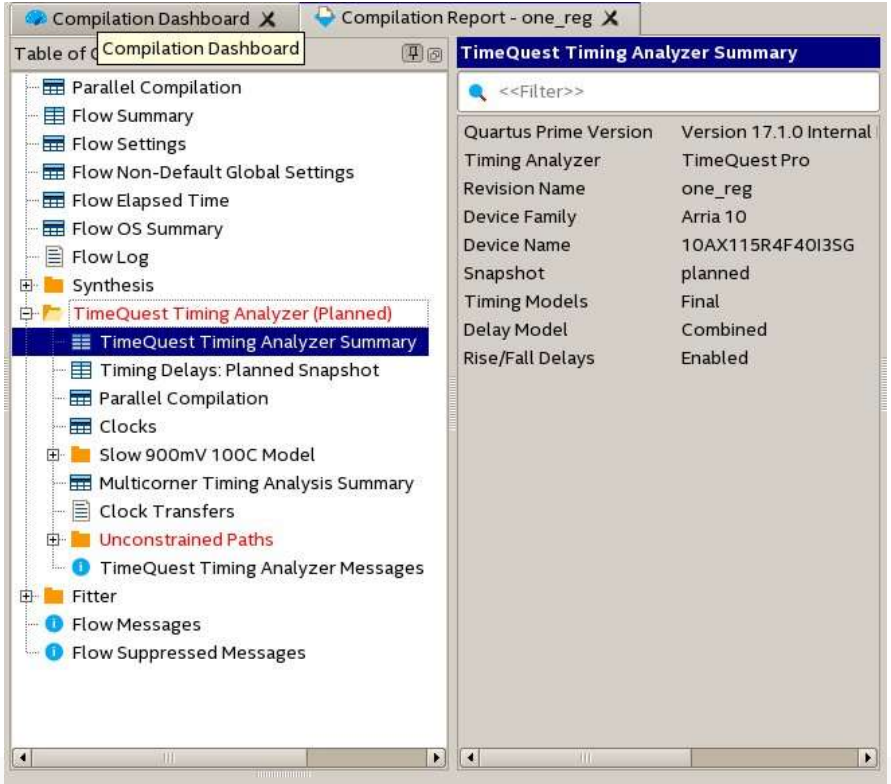
We asked the Tools Specialist Application Engineers:

“What are the causes of delays in debug and deployment?”

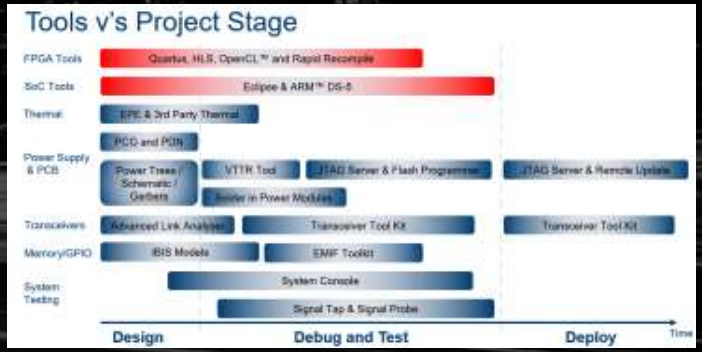
1. Customer doesn’t close timing (goes straight to hardware)
2. Customer doesn’t review Critical Warnings
3. Customer doesn’t read any Warnings
4. Pins not fully constrained
5. Timing constraints not complete, or applied everywhere

Timing Analyzer Snapshot Reports

- Timing Analyzer Reports based on snapshots
- On by default
- Viewable during flow



ARM DS-5 Intel SoC FPGA Edition: Debug Advantage



FPGA-Adaptive Debug

How do I develop embedded SW interfacing to an FPGA?

Drivers?

Optimize?

Debug?

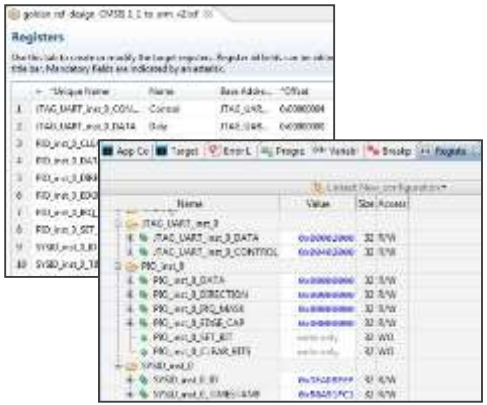
FPGA-Adaptive Debug

Driver?

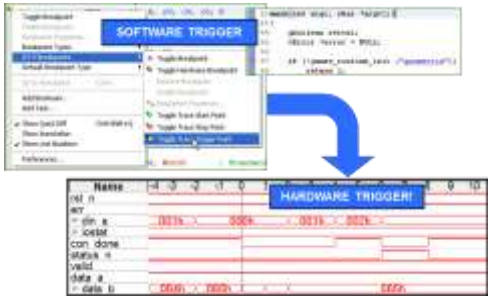
Optimize?

Debug?

Register views of FPGA peripherals



Cross triggering and global time stamping



ARM DS-5 Streamline Performance Analysis

ARM DS-5 Intel SoC FPGA Edition: Overview

- ARM - Intel FPGA strategic partnership with unique OEM arrangement
- Complete multi-core debug and ARM CoreSight compliant trace
- Includes ARM compiler and Intel FPGA GCC compiler
- Industry-only FPGA-Adaptive debug support
- Low cost, included in Intel SoC development kits

ARM DS-5 Intel SoC FPGA Edition: Debug Features

Standard Software Debug Interface

- Intuitive with no relearning.

FPGA Adaptive Debug

- Easy Cross-trigger setup
- Visually correlate hardware and software events

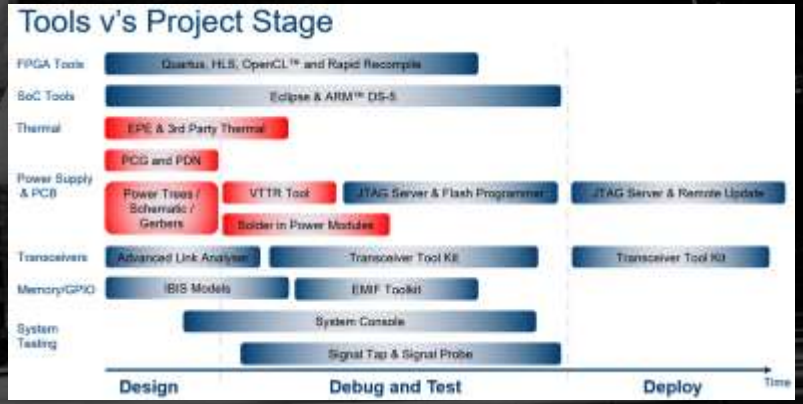
System Trace Module Support

- Easy setup of STM
- Superior visualize of processor trace

Low Cost Debugging

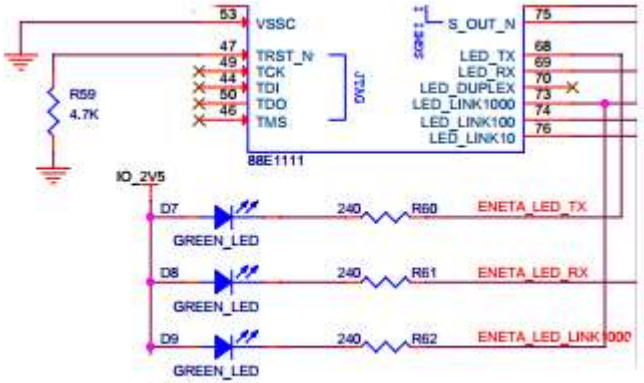
- Intel FPGA Download Cable (USB Blaster II) for low cost debug
- ARM DStream for advanced debug capabilities

Power & PCB Tools



PCB and Power Tools

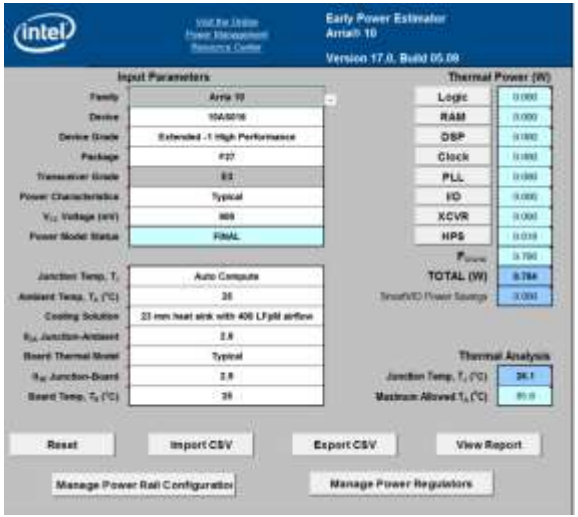
> Schematic Diagrams of Intel Devkits
  > Freely available on development kit pages
> Pin Connection Guidelines
  > What voltage on which pin, any sequencing?
> Early Power Estimator
  > How much power do I need to supply?
> Power Distribution Network Tool
  > Have I got enough decoupling?



Early Power Estimator (EPE)

- Early Power Estimator is a spreadsheet (macros enabled)
  - Entered manually or with Compilation Results
  - Produces:
    - Power Estimate
    - Thermal Analysis based on entered data
- Benefits
  - Allows you to analyze power budget for your board before your design files are available
  - Provides a rich modeling environment with reliable accuracy where you can perform what-if scenarios and check your assumptions

Input
Resources used
Clocks and Frequency
Transition Rates
Temp, Air Flow, Heat Sinking



Reports
By Resource
By Supply
Thermal Analysis

Quartus® Power Play Power Analyzer

> More accurate than Early Power Estimator (EPE)
  > Considers exact routing used

> Benefits
  > Provides highest post-fit power estimation accuracy with Altera's advanced modeling technology
  > Generates detail power estimation analysis

- Has a push-button automatic power optimization with no change to your design flow
- Has a build-in power optimization advisor providing suggestions and information to minimize power consumption

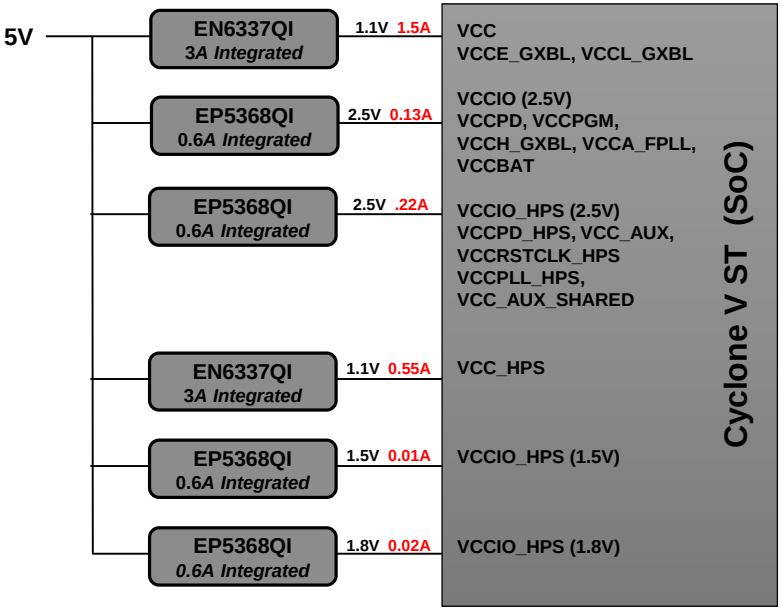
Input
Number of Registers
Transition Rates
Clocks and Frequency
I/O and Memory
DSP and PLLs
Temp, Airflow, Heat Sinking
Simulation Results
Place-and-Route Results
Node Activity

Power Analyzer

Reports
By Resource
By Supply
Thermal Analysis
Confidence Metrics
Signal Activity Data

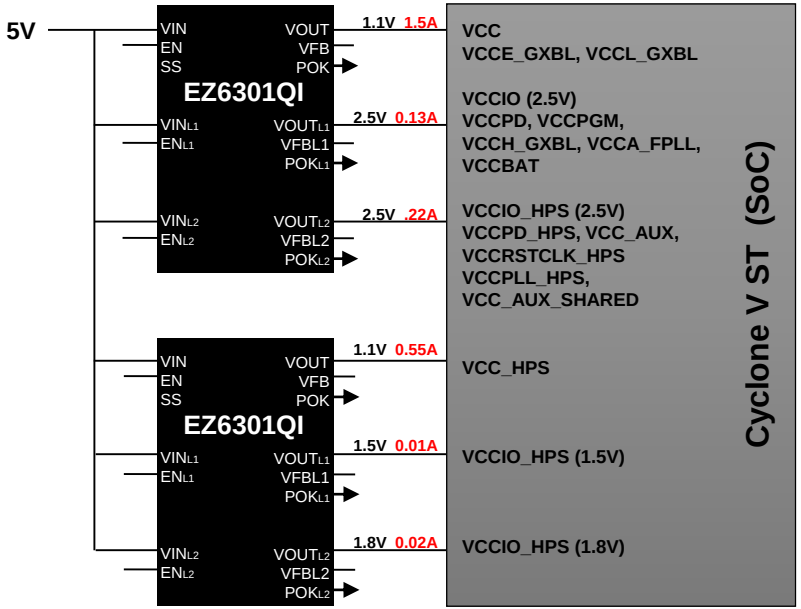
Intel Power Trees - Cyclone V SoC

Traditional Approach

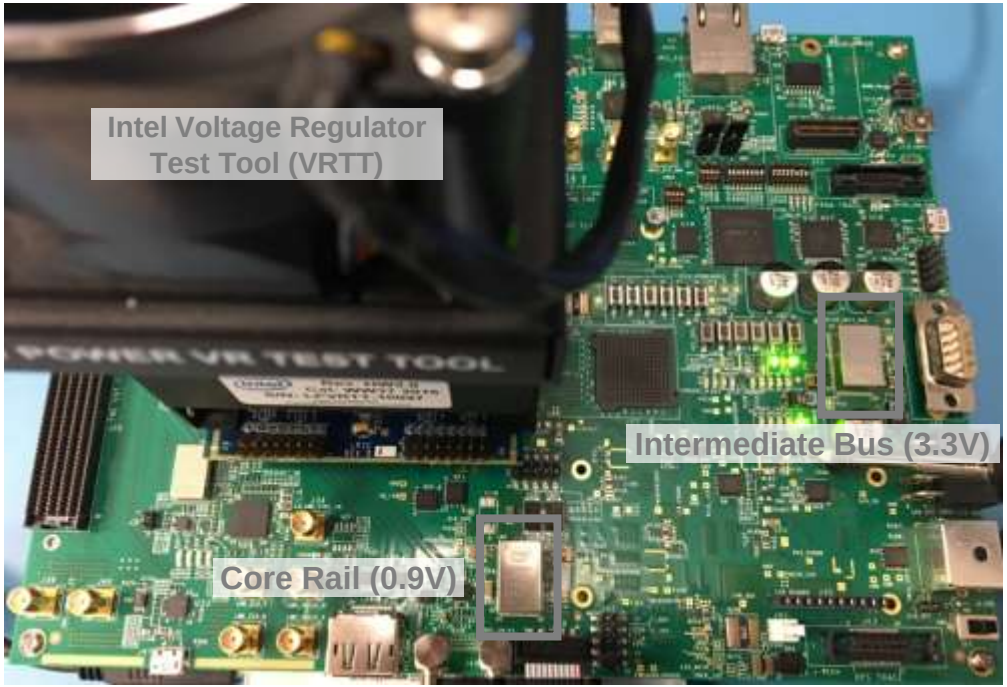


Note: Ferrite Beads are not shown

Now Even Easier with EZ6301



Using Intel® VRTT Test Tool



Enpirion Drop-In Boards

1. Remove on-board power supply from PCB
2. Connect VIN, VOUT, and GROUND pins on drop-in board with wires to PCB
3. Begin testing new power solution right away!

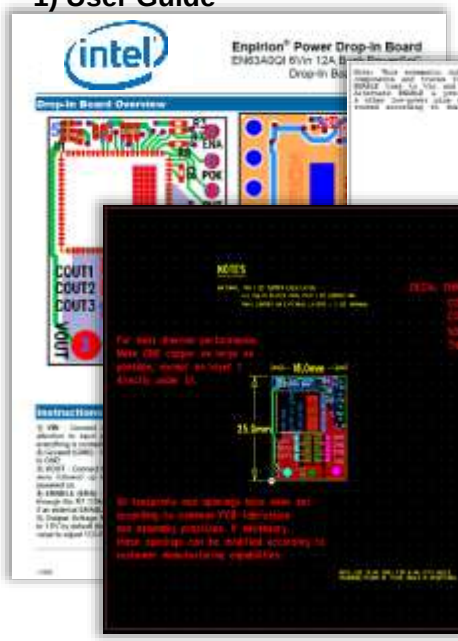
Just *Drop In* and Go!

See on Booth

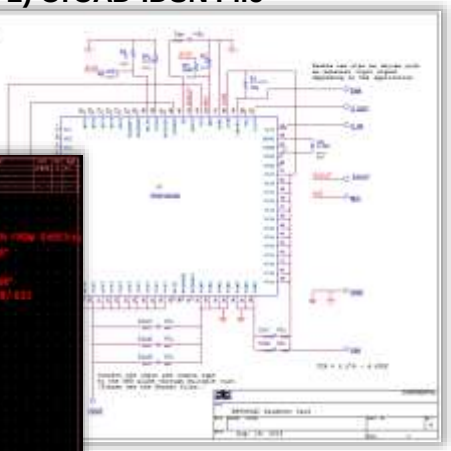
Drop-In Support Packages

- > Comprehensive User Guide
- > Complete Design Package
  - > .DSN file
  - > PADs and ASCII layout files
  - > Gerber file
  - > Application notes

1) User Guide

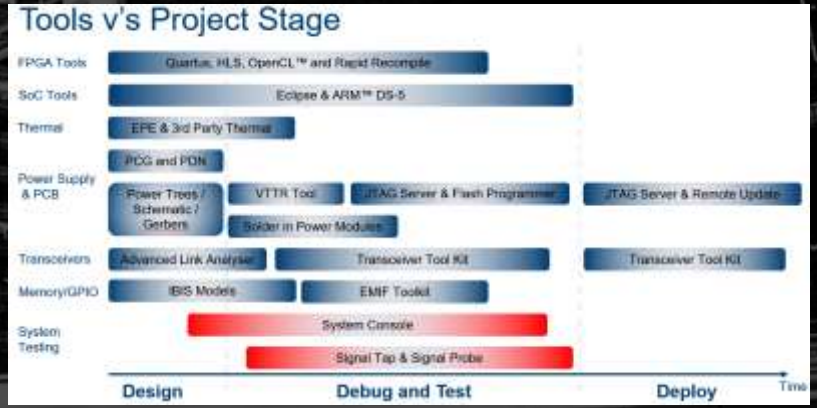


2) OrCAD .DSN File



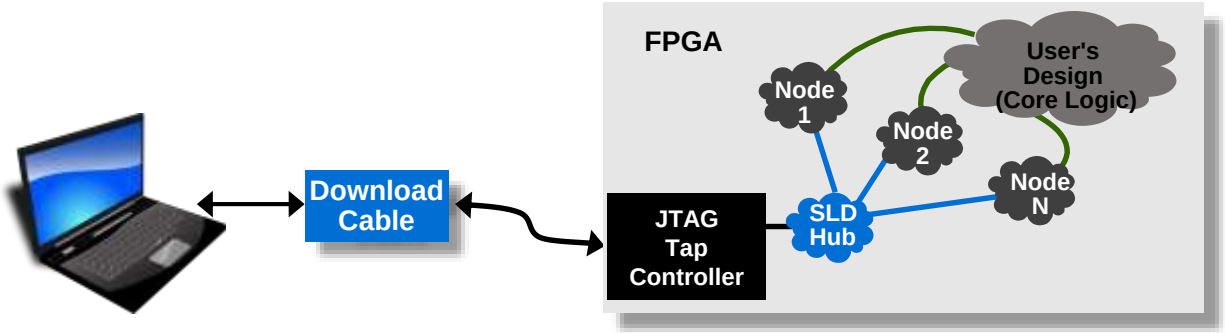
3) PADs .PCB and GERBER files

On-Chip Debug



On-Chip Debug Technology

- Debug tools communicate with the FPGA via standard JTAG interface
- Multiple debug functions can share the JTAG interface simultaneously
  - Intel's system-level debugging hub technology makes this possible



On-chip Debug Tools in Quartus Prime Software

- Signal Probe
  - Quickly routes an internal node to a pin for observation
  - Does not use SLD technology due to nature of tool
- Signal Tap logic analyzer
  - Captures and displays hardware events, fast turnaround times
  - Incrementally creates trigger conditions and adds signals to view
  - Uses captured data stored in on-chip RAM and JTAG interface for communication
- In-system memory content editor
  - Displays content of on-chip memory
  - Enables modification of memory content in a running system
- External logic analyzer interface
  - Uses external logic analyzer to view internal signals
  - Dynamically switches internal signals to output
- In-system sources and probes
  - Stimulate and monitor internal signals without using on-chip RAM

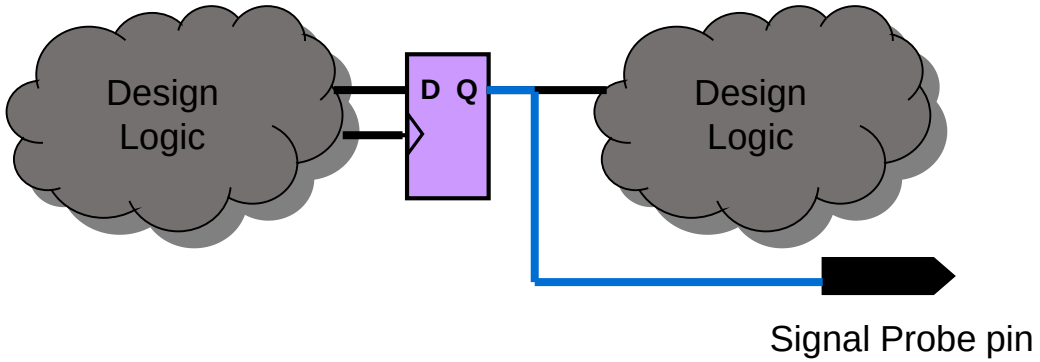
Signal Probe

> Signal Probe is designed to provide access to internal nodes when debugging an FPGA in a lab

> Quickly routes an internal node to a free external pin for observation

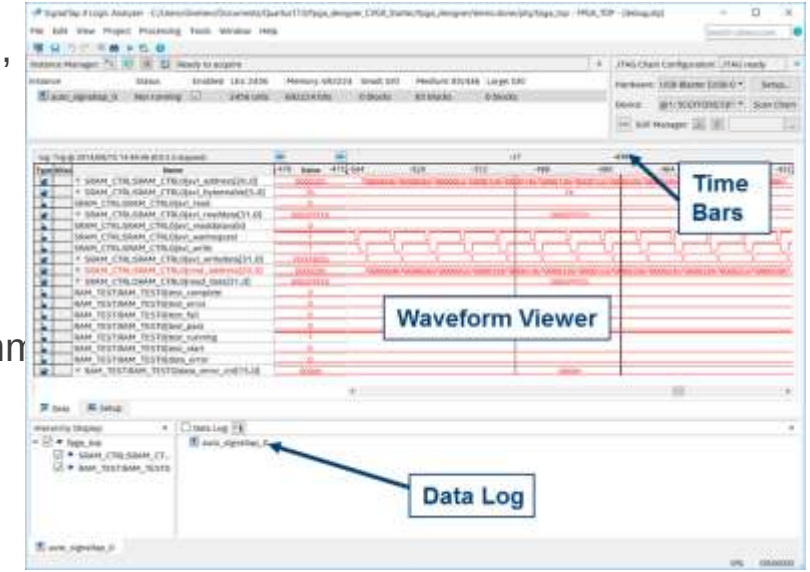
> Signal Probe pins are routed in the post-fit design

- Minimal to no impact to existing fit, route and performance



Signal Tap Embedded Logic Analyzer

- Full featured “Soft” Logic Analyzer
  - Wide range of triggering options, storage qualifiers,
  - Data log – capture in lab, analyze later
- Most signals are visible
  - Exception – Hard IP blocks, some IO functions
- Large signal sets are not a problem
  - Signal Tap instances with 500-700 signals are comm
- Available for Free
  - Installed with Prime, Standard or Lite Editions
  - Installed with Stand-Alone Programmer



Utilizes Intel Rapid Recompile for Probe Changes

Signal Tap Resource Utilization

- Signal Tap Uses Device Resources for Implementation
  - ALMs/LEs for logic analyzer function and JTAG communication
  - Memory for sample storage
- Resources used depend on several factors
  - Number of signals monitored and included in the trigger enable
  - Number of trigger levels defined
  - Capture Depth (64 to 128K)
- Example
  - Cyclone V, 169 channels (11 enabled for trigger), 4K capture depth
    - 2500 LEs (506 ALMs, 1460 FFs, 85 M10K block RAMs).

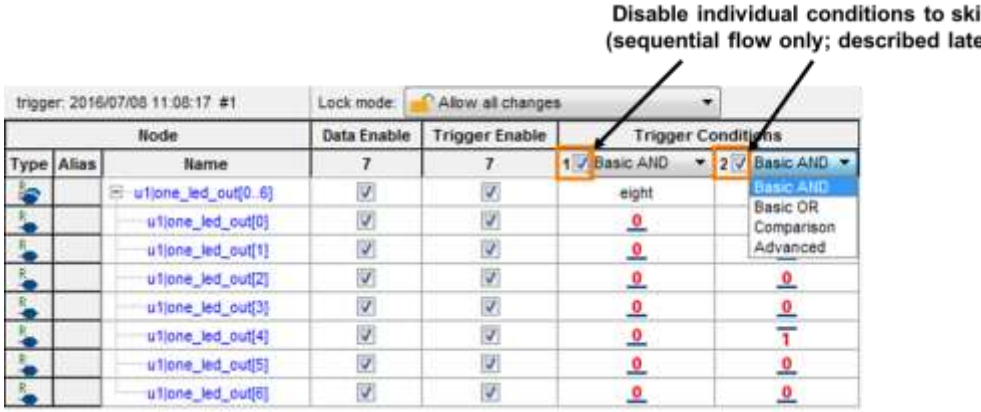
Triggers and Buffers

Basic AND: *all* signal levels/transitions must be true

Basic OR: *any* levels/transitions true; bits in groups are OR reduced unless condition is a numerical value

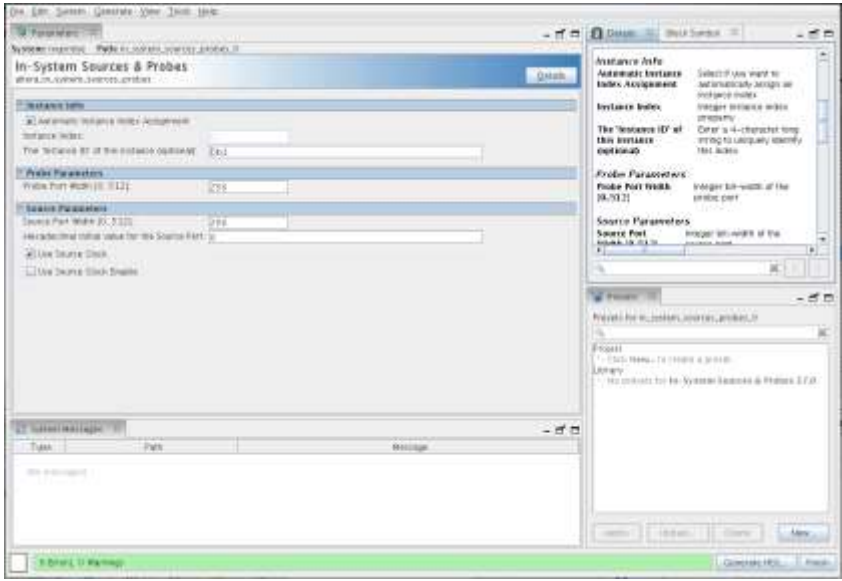
Comparison: extension of **Basic OR**; compare groups to expected integer value(s)

Advanced *(details in training presentation)*



In-System Sources and Probes IP

- Provides in-system debug by stimulating and monitoring internal signals
  - Can be used to force hard-to-reach trigger conditions
- Main components
  - In-System Sources and Probes IP core – Create instance
  - In-System Sources and Probes Editor – Read probes and write source values



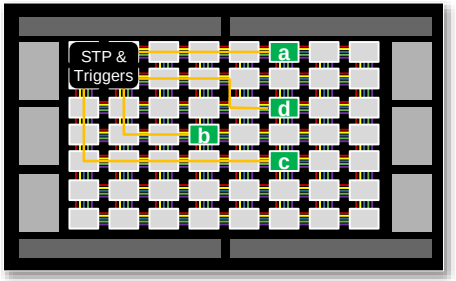
Post-Fit Signal Tap with Incremental Route

> Faster Debug Iterations with Stratix 10

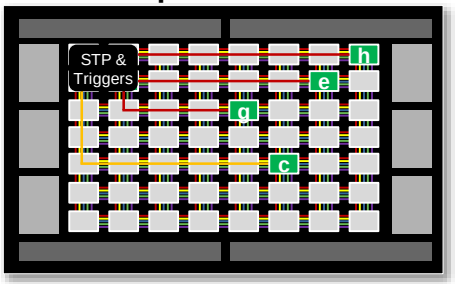
> Change Signal Tap probe points without re-compile

- > Signal Tap with timing preservation
- > If only probes change, only incremental route needed

Signal Tap Probes Post-fit

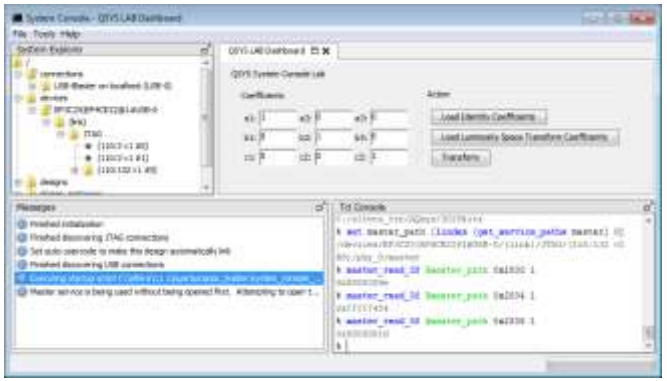


Rapidly change Signal Tap Probes

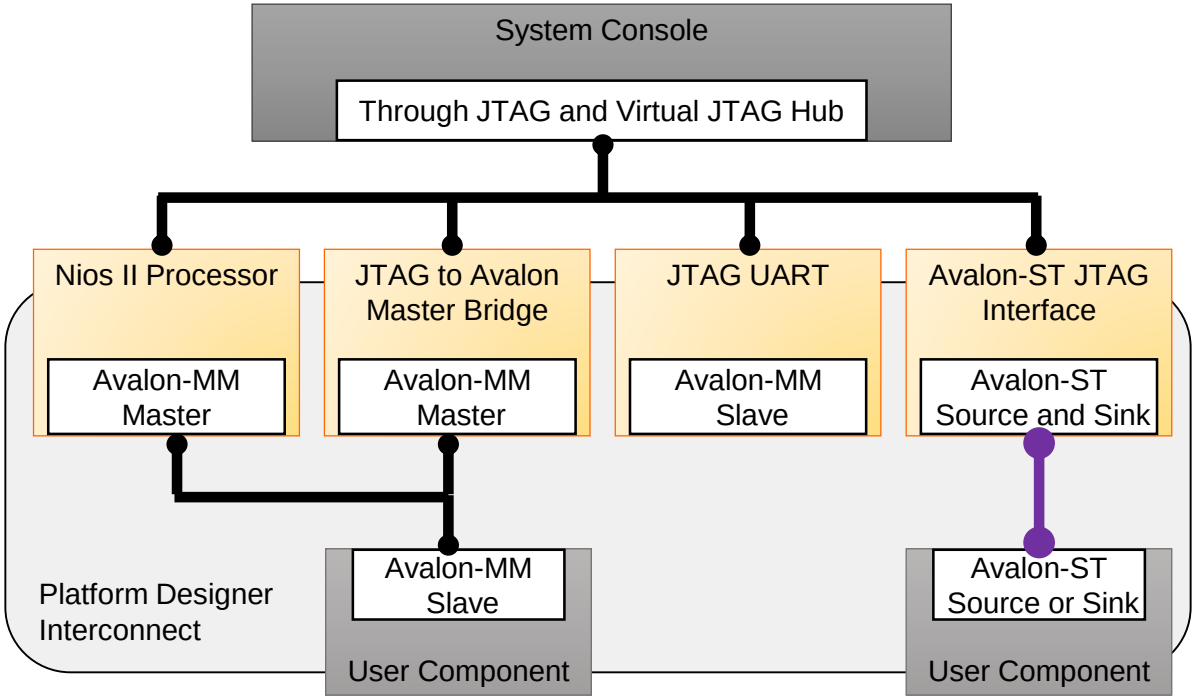


What is the System Console?

- Quick system-level debug of Platform Designer (QSys) systems
  - Interactive Tcl Console
    - Opens as a separate window
    - Opens in the Nios® II Command Shell
  - Debug over various communication channels
    - JTAG or TCP/IP
  - Read from or write to memory mapped components
  - No processor required
  - Add widgets to “your” GUI to monitor and control



System Console Interfaces



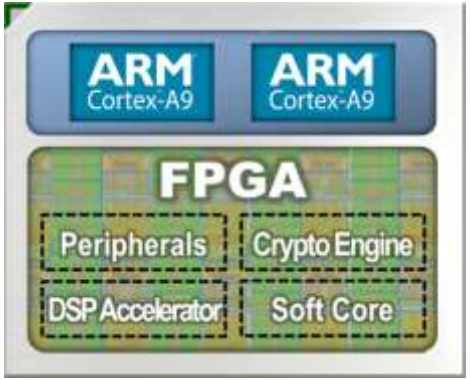
Usage Examples

- System-level debug
  - Board bring-up and interface testing
  - System clock, reset and JTAG chain validity testing
  - Platform Designer component functionality testing
  - Loopback testing of Avalon® Streaming interfaces
  - Provide test vectors, return responses
- Other Uses
  - Transceiver Link Debug
  - Debug External Memory Interfaces

Processor Aided Debug

Can the processor aid board bring up?

> Integrated processors can bring benefits to board bring up
  > Processor is tightly coupled
  > Can reconfigure the FPGA
  > Processor system is “known good” (dependent on your PCB)
  > **Can act as a bridge to debugging tools**



CPRI

Ethernet

OS

Server

Custom Applications

Debug Hub

Logic

Logic

FPGA Programmable Logic

- SoC FPGAs can run an Operating system - Eg Linux, VxWorks
- OS can provide a network socket that acts as a JTAG server
- External remote access to the device anywhere on the private network (can be authenticated). Remote access to Signal TAP anywhere in the world!
- Application Note 693 has more detail

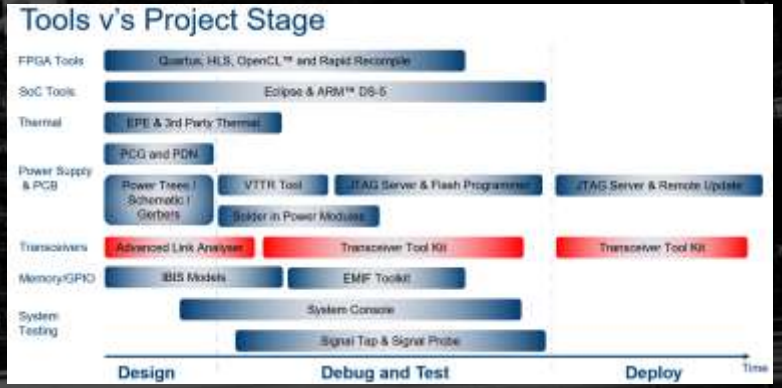
Remote Hardware Debugging over TCP/IP for Altera SoC

2015-05-11

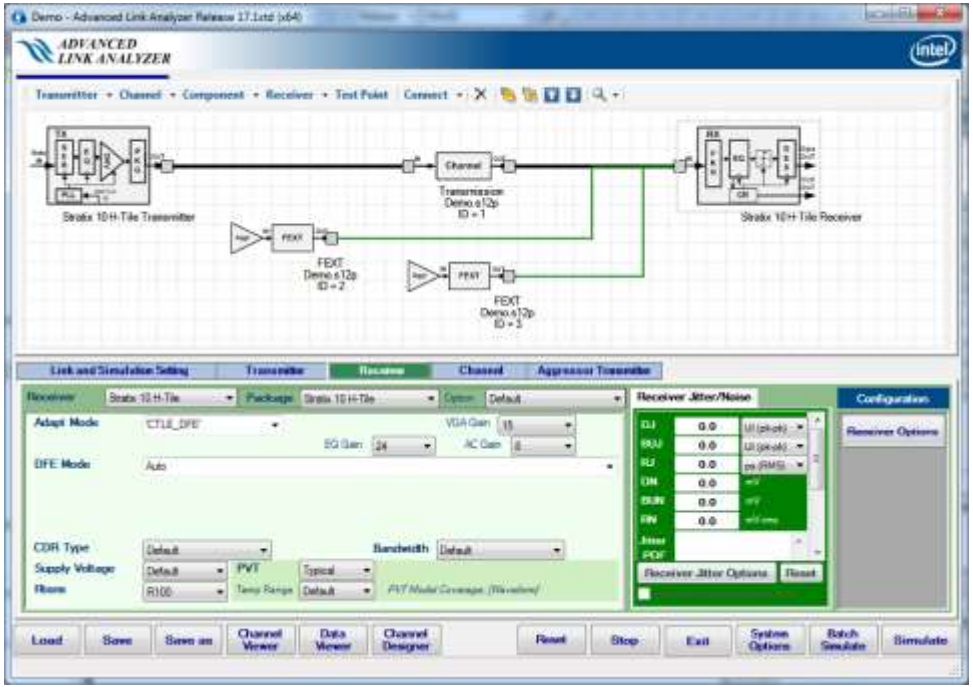
AN693 Subscribe Send Feedback

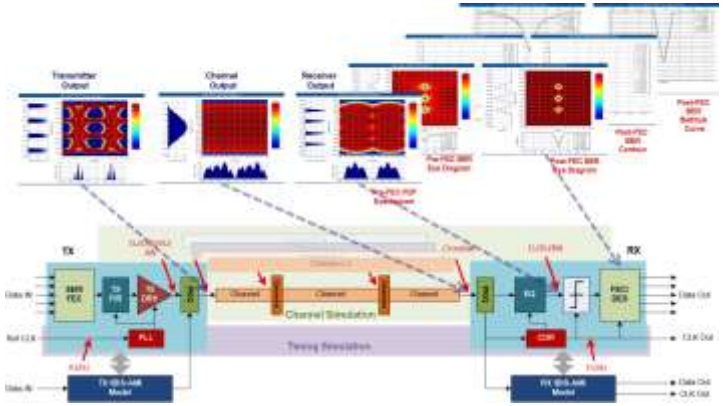
You can perform remote debugging of your system with System Console. Debug equipment deployed in the field through an existing TCP/IP connection. Run a network stack on either a Nios II processor or a hard processor system (HPS) and piggyback on an existing remote administration setup. This application note focuses on the case of using an Altera SoC.

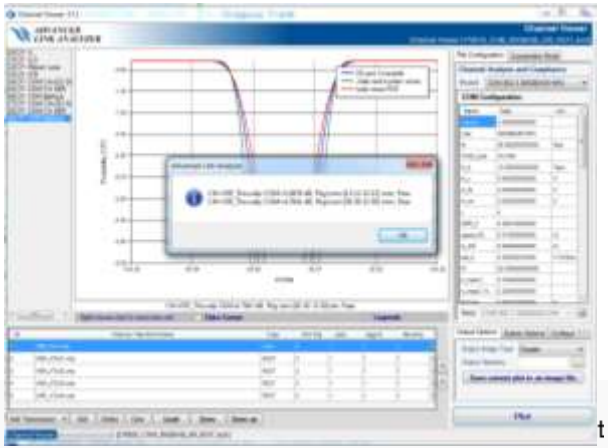
Transceiver Tools



Intel® Advanced Link Analyzer – (JNEye)

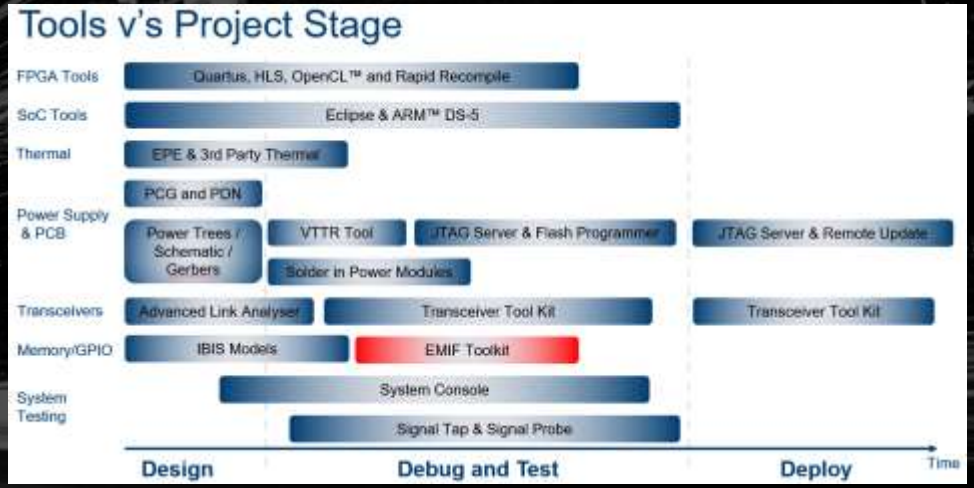






https://www.altera.com/education/demonstrations/transceiver-toolkit/transceiver-toolkit-demo.html

EMIF Toolkit

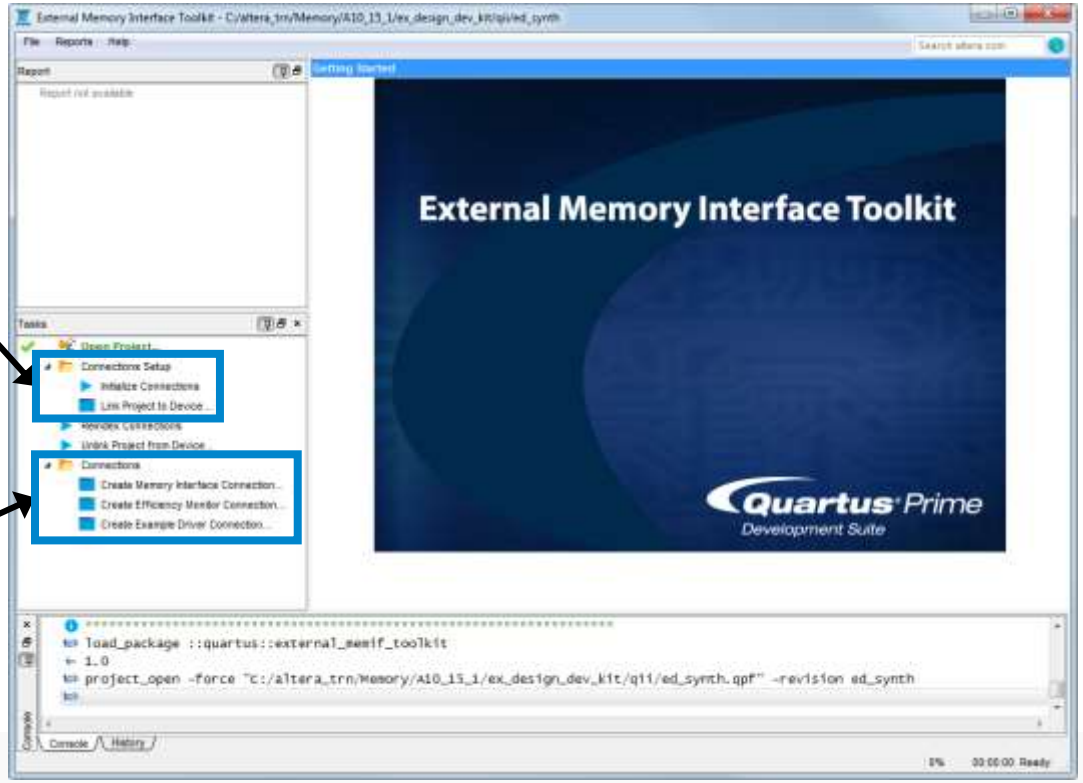


EMIF Debug Toolkit in Action

Quartus **Tools** menu → **System Debugging Tools**

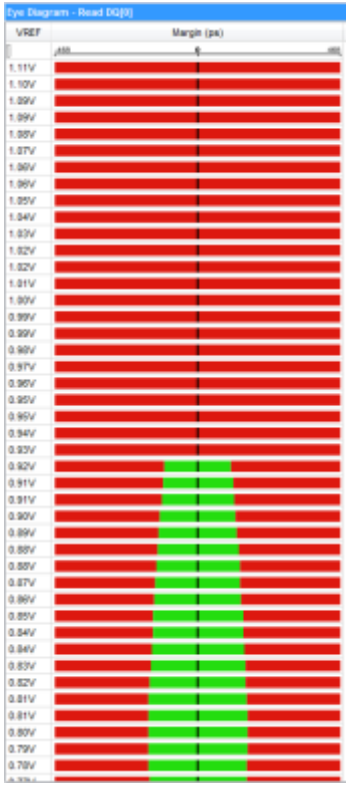
Establish connection to device and link to design

Connect to EMIF for using tools and report generation



External Memory Interface Debug Toolkit

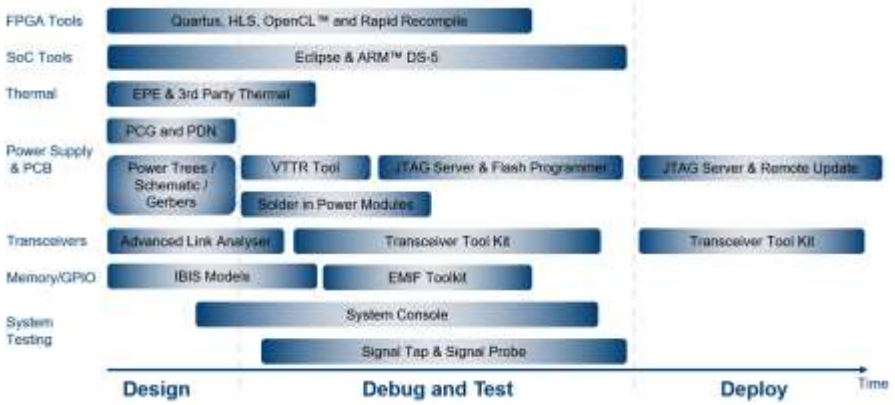
- Analyze results of calibration
- GUI and Tcl task/report interface, similar to Timing Analyzer
- Report on calibration status and selected settings
- Margining activities
- Generate and save reports on calibration and margins
- Manually recalibrate interface at any time
- Read selected calibration settings and adjust individually
- Provide statistics on the data transfer efficiency of the interface
- Connects to debug port of Nios® II-based calibration subsystem (I/O AUX)
  - Avalon®-MM slave interface



Summary

> Debug & Test is a time-critical stage

- Several Tools are available to help
- Training is readily available on-line
- Time invested in learning these tools pays for itself many times over in shorter debug cycles



Invest Time Now & Save Time Later