Welcome to FPGAworld Conference 2018
Stockholm 18 September and Copenhagen 20 September

The FPGAworld Conference is an international forum for researchers, engineers, teachers, students and hackers. It covers topics such as complex SW/HW embedded systems, FPGA based products, educational & industrial cases and more. The academic & industrial tracks at FPGAworld, meals, premises, administration etc. is paid for by industry sponsors and exhibitors.

Following types of contributions:
Contribution A – Industrial or Hackers presentations, with focus on industrial or hackers projects/applications. It is not allowed with marketing a product for profits (product presentation).
Contribution B – Student presentations of projects selected by the Academic Student Program Committee (call for papers).
Contribution C – Product presentations
Contribution D – Industrial and academic tutorials (1,5-3 hours, Stockholm)
Contribution: Student Sponsoring – To enable students from all over the world to present their work on FPGAworld
Contribution: Booking for Exhibitors and FPGAworld Sponsors – please contact Mia (mia.lindh [at] fpgaworld.com)
Contribution: New Industrial Program Committee Members – please contact Lennart (lennart.lindh [at] fpgaworld.com). Gets inside information and also the opportunity to influence the industry program.

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Contents

Keynote Speaker 2018, Stockholm and Copenhagen

Pieter J. Hazewindus, Synopsys, Mountain View, CA

Title: Advanced Verification and Debug for Large and Complex FPGA Designs

Abstract: The FPGA industry is in a period of rapid change. There has been a significant growth in size and complexity of FPGAs with each new generation. This has given rise to several challenges to FPGA design which are now needing a more ASIC "like" design methodology. We survey the implications for designers implementing FPGAs, IP designers, as well as the tools supporting the FPGA designs.
With the introduction of FinFET technology-based FPGAs, single-FPGA design sizes have taken a big leap, while the maximum operating frequencies have increased, and the power consumption has decreased dramatically. FPGAs have become more feasible as replacements for ASICs, and as stepping stones towards eventual ASIC implementations. The scale of integration challenges traditional testing methods, such as simulation. More complex clocking schemes require enhanced verification methodologies. And RTL debug of a multi-million gate FPGA design in reasonable time necessitates novel strategies.
Pieter Hazewindus leads the development of software solutions for the implementation of FPGA designs as well as ASIC prototyping on FPGAs at Synopsys. He is responsible for the Synplify Pro and Premier family of products, which have provided synthesis support for FPGA vendors since 1994. Prior to Synopsys, he held both managerial and software developer positions at Synplicity, Cogit Corporation, and Mentor Graphics. Hazewindus holds a Ph.D. in Computer Science from the California Institute of Technology and an M.S. in Mathematics from the Eindhoven University of Technology. More; https://www.linkedin.com/in/graham-copperwheat-5991755/

Keynote Speakers 2018, Stockholm

Graham Copperwheat – Intel PSG located in UK.

Title: FPGA – The Multifunction Accelerator of ChoicePGA

Abstract: Recently, we're living in an increasingly smart and connected world, a world that is generating increasing amounts of data and driven to find new ways to extract value from this data. A world that needs technology solutions that can not only meet today's demands but also tomorrows. FPGAs are stepping up to meet this challenge by writing the next chapter in the story of their evolution – FPGA as a reconfigurable multifunction accelerator. What are the characteristics of this new chapter, what are the strategies the FPGA industry is deploying to address the demand?

More about Graham Copperwheat see: https://www.linkedin.com/in/graham-copperwheat-5991755/

Keynote Speakers 2018, Copenhagen

Hichem Belhadj, Chief Systems Architect – CTO Office, Microsemi Corp. USA

Title: Artificial Intelligence and the Use of Programmable Technologies

Abstract: Recently, Artificial Intelligence (AI) went from hype to become reality as platforms and eco-systems that incorporate artificial intelligence gain ground in many sectors such as Ad targeting and E-commerce, traffic and network analytics, Insight-driven financial transaction, clinical analytics, and autonomous factories. In this keynote, we will review the underlying hardware and eco-system architectures enabling machine learning, cognitive computing and other advanced analytics technologies. A review of the various hardware processing capabilities (GPUs, CPUs, FPGAs) and how they are pooled and harnessed broadly to accelerate computational workloads. The review will also cover the much-needed eco-system to enable many more applications and a broader community of users. At the end, we will introduce an exploration of which architecture fits what workload.

Hichem Belhadj has been with Microsemi for close to 20 years. He is currently the Chief System Architect at the CTO Office. Prior to joining the CTO Office, Hichem held executive management positions in Corporate Sales and Field Systems and Applications at Microsemi, Actel, IST, and INPG. Hichem holds a Master and PhD from the Polytechnic Institute of Grenoble, France. More; https://www.linkedin.com/in/hichem-belhadj-43b6792/

Contribution A – Industrial or Hackers presentations, with focus on industrial or hackers projects/applications selected by the Industrial Program Committee

Low Cost OpenCL Acceleration For Science And Engineering Projects

Abstract: A presentation examining the use of low cost Cyclone-10 hardware platforms and OpenCL programming to accelerate the processing of scientific and engineering data processing algorithms. This presentation examines the benefits and pitfalls of an OpenCL approach using FPGA technology to supplement software data processing techniques.
Length: 20 min
Event: Stockholm, Copenhagen

John Adair, UK and Enterpoint

How Formal Techniques can keep hackers from driving you into a ditch

Abstract: The dark side of our connected future is here. From the comfort of a living room sofa, security researchers were able to remotely disable the brakes and transmission of a new Jeep Cherokee — literally driving the vehicle into a ditch. Traditional approaches like expert inspection, functional testing, and teams of white hat hackers are not finding the holes attackers are exploiting. So what can be done to prevent this? Two words: Formal Verification.
Formal verification is a fundamentally different approach to other functional simulation techniques. It comprehensively and exhaustively proves the validity of an assertion for all state space in a design. In the past formal verification required engineers to under SystemVerilog properties and assertions to harness its power, but formal apps like Mentor's secureCheck bring this technology to the masses. SecureCheck allows users to easily prove isolation of design paths. For example to prove that there is no way a passenger could access the vehicle control system through a USB port use for entertainment devices. Or that there is no way to access the private key storage through and AXI bus that could be manipulated by a processor on an FPGA SoC. In short it is an application that keeps the bad guys out of the places you don't want them. When there is a vulnerable path in it provides a counter example waveform showing how a hacker could gain access to the protected areas. SecureCheck is a proven technology that has many years of customer use. It has prevented critical vulnerabilities from getting into products for major companies throughout the industry. In some cases it has been use retroactively to understand how hackers have gained access and then plugged the hole. Learn about this technology and how you can use it on your next project to keep things secureLength: 30 min
Stefan Bauer, Germany and Mentor - A Siemens Business

Stockholm and Copenhagen

Use Vertical Integration in industrial applications with Programmable System on Chip

The higher the automation, the higher the productivity. There are gains to be had from having access to information from every unit that contributes to your automation application. However when combined with the processing power of state-of-the-art controllers, and the acceleration provided by the FPGA logic, this enables the implementation of algorithms which previously were difficult or even impossible to implement. The Industrial Internet of Things (Industrial IoT) promotes the right technologies, protocols and interfaces and is accelerating the need for this increased automation and productivity improvements.
This presentation will explain how to use Xilinx Heterogeneous Multicore devices as a fully integrated device in Industrial IoT solutions. The combination of PLC runtime functionality in the Processing System, in tandem with industrial communication that interconnects all nodes in an industrial IoT application will be demonstrated. A special focus will be put on how Time Sensitive Networking (TSN) can already be used today in this context. You will also see how advanced design methods like High Level Synthesis and powerful tools such SDSoC C/C++/OpenCL full-system optimizing compilers, can be used to quickly and effectively create high performance automation applications.
An overview of reference designs and demonstration platforms will complement this talk.
Length: 30 minutes

Event: Stockholm, Copenhagen
Magnus Lindblad <magnus@xilinx.com> **and** Ole Hojrup <ohojrup@xilinx.com>

Scoreboarding

There is a lot of talk about scoreboards for FPGA (and ASIC) verification. This presentation will present some different angles on this subject and show how this can be done for relatively simple testbenches, and also for more advanced testbenches, all examples using straight forward VHDL and open source libraries. The planned ESA (European Space Agency) sponsored UVVM extensions will also be presented.
Length: 30 min
Event: Stockholm
Espen Tallaksen, Norway and Bitvis

Deep learning application on edge FPGAs

Realtime decision making for autonomous control systems suffer greatly from the latency addition introduced when trying to move such applications to the cloud. Edge based decision making algorithms, such as Deep learning, is a potential candidate for improvements by performing on site filtering. In this work we have explored the possibility to employ a FPGA SoC for running deep learning algorithms on the edge. The results show capability of accurate and realtime performance while maintaining a low power consumption.
Length: 30 min
Event: Stockholm
August von Hacht, <august.von.hacht@synective.se>

Country: Sweden and Synective Labs AB

More information: The implementation runs a binary neural network on a zynq 7020 which will be demostrated after a presentation of the full system.

Adaptive Design of Optimized Deep Neural Networks for Embedded Systems

Abstract: Deep Neural Network (DNN) has already revealed its learning capabilities in runt-time data processing for modern applications. DNNs are ever-evolving, and complex processing models

containing up to millions operations for the entire model which make their implementation overwhelming. To tackle DNN hardware implementation challenges on embedded systems, we propose an automatic framework aiming to simplify the load complexity of DNNs by designing a highly robust DNN architecture by taking advantage of a multi-objective evolutionary approach.

Event: Stockholm

From: Mohammad Loni, <mohammad.loni@mdh.se>

Country: Sweden and Mälardalens University

More information: The framework takes advantage of a multi-objective evolutionary approach, which exploits a pruned design space inspired by a dense network. The proposed framework considers the network size and network validation accuracy factors to build a highly optimized network fitting with limited computational resource budgets of embedded platforms while delivering comparable accuracy level.

Optimized Deep Learning on FPGAs

Abstract: FPGAs offer several advantages for use in the field of deep learning in terms of power, stability and performance. However, current frameworks sacrifice considerable performance in favour of flexibility when used for FPGAs.
The presentation deals with the advantages of implementing deep convolutional networks that are specifically designed for FPGAs. It does so by outlining methods for optimally using the FPGA resources by employing techniques such as bit-width reduction and 1-bit weights.

Length: 30 min

Event: Stockholm

Table: no

From: Yasser Kilde Bajwa, <yasser@grazper.com>

Country: Denmark and Grazper Aps

Pistonhead – A BroadR-Reach camera for the automotive industry

It is a camera which outputs video over a BroadR-Reach link. BroadR-Reach (also known as 100BASE-T1 or IEEE 802.3bw) is an automotive Ethernet standard for vehicles. It uses a different physical layer than classic Ethernet, but protocols look the same.
BroadR-Reach uses a single unshielded twisted pair cable for 100 Mbit/s full-duplex point-to-point communication. This reduces cable weight, cable cost and requires less space for cabling, compared to classic Ethernet.

Event: Stockholm

From: Niclas Jansson [mailto:niclas.jansson@bitsim.com]

Bitsim, Sweden

Contribution B – Student presentations of projects selected by the Academic Student Program Committee

Face Detection and Recognition with PYNQ FPGA & Python Programming

In this paper, face detection and recognition algorithm is discussed. Haar cascade algorithm is used for face detection, and local binary pattern (LBP) algorithm for face recognition. Haar cascade classifier extracts the features from the image. For all feature images, the best threshold are found and then the positive and negative image is easily classified. Thus the detected face is cropped and stored on a dataset which will be trained. The image is saved in sequenced order of ID and sample number. LBP algorithm divides the image into several parts to extract the binary pattern. Features obtained from zone are concatenated into signal feature histogram, a form of an image. Comparing by measuring between their histogram. Image is trained and gets ID number of a face, which recognizes the face. The trained image is saved on the extension of yml/XML. The Classification and Recognition algorithm has been implemented on the PYNQ FPGA hardware in Python programming environment. There is a need of a huge dataset of the face, with their variation in a human face area in term of size, pose & experience.

Length: 20 min + poster session

Event: Stockholm

Krishna Gaihre, Institute of Engineering, Pulchowk Campus/Tribhuvan University, Nepal

Audio Signal Distortion with FPGA

The project is a real-time signal processing project that intends to create an audio effect called distortion, implementing it with field-programmable gate arrays (FPGA) devices. The distortion described in this project and the one related with communication systems are somewhat related but are different; different in the sense that distortion is generally considered unwanted but in this project is intentionally used as an effect. It is designed using VHDL and uses both the behavioral and the structural flow of design. It is implemented with a Spartan-3E Starter Kit using Xilinx ISE. The project is designed to distort the real-time signals referencing a twenty-two fretted standard tuned guitar. VHDL modules are designed which take audio signal through the onboard ADC, process the digital data and generate the output through the onboard DAC. In addition to the FPGA devkit, the project utilizes a dual power supply, a pre-amplifier and an analog filter as mandatory requirements for the successful completion of the project.

Length: 20 min + poster session

Event: Stockholm

Frank Shrestha, Khwopa Engineering College, Nepal

Implementation of AES Encryption and Decryption in FPGA for Wireless Data Transmission

This paper proposes secure wireless transmission of text message by implementing Advanced Encryption Algorithm (AES) in FPGA. Coding is done in VHDL. The encryption and decryption algorithms are implemented on two separate Spartan 3E boards. One board acts as transmitter, where text message of 16 characters is encrypted using key of same length and is transmitted wirelessly. Another board acts as receiver, which decrypt the received message to obtain original text message. This design needs key at transmitter and receiver both sides. Simplex communication mode is established between two devices.

Length: 20 min + poster session

Event: Stockholm

Rukesh Prajapati, Khwopa Engineering College, Nepal

Data Type Agnosticism with Academic and Commercial High-Level Synthesis Tools

In the field of Electronic Design Automation (EDA), high-level synthesis (HLS) is an automated design process that brings a significant reduction in design cycles by pushing the design to the higher levels of abstraction with the use of high-level languages (HLL). This paper presents the implementation of an algorithm namely Sum of Squared Differences (SSD) with high-level synthesis in connection with a data type-agnostic programming methodology which makes the implementation even more adaptable. Recently, it was shown that a data type-agnostic programming methodology empowers Xilinx Vivado HLS to synthesize digital architectures for a plethora of data types without modifications of the C source codes. Especially, the very same code can be used for real-valued and complex-valued data paths by utilizing the C++ class and template system. Taking it further, five more HLS tools were used to implement the aforementioned methodology. Along Xilinx Vivado HLS the other five tools used were namely Mentor Graphics Catapult, Intel HLS, LegUp, Kiwi, and Bambu. The HLLs used were C, C++ and C#.

Length: 20 min + poster session

Event: Stockholm

Babar Khan, University of Bremen, Germany

Contribution C – Product presentations

Staying Competitive with modern FPGA Verification Methodologies (part 1 and 2)

FPGA vendors continue to push the boundaries creating innovative new ways for users to efficiently design into today's increasingly complex FPGAs. Recent industry surveys show a direct correlation between a designs complexity and a program's inability to deliver a working FPGA on schedule. Additionally, time spent in verification is trending upwards while simultaneously, an increasing number of costly bugs are not being found until before going to production. This presentation arms

engineers with the advanced verification methodology they need to deliver working designs within a predictable schedule in today's quickly evolving FPGA market.

Advanced verification is a broad topic with many diverse areas. This presentation focuses on four main areas:
• Automation enables engineers to focus on the important, and honestly more fun, tasks while leaving the boring repetitive tasks like test bench creation and parsing through test results to a computer.
• Verification IP lets engineers avoid sinking valuable time writing and debugging models or BFMs for industry standard interfaces and become immediately productive exercising the custom logic that needs it.
• Formal verification apps targets critical time consuming tasks where traditional functional simulation falls short. Formal verification technology is fundamentally different approach that enables comprehensive and exhaustive verification without the need for any test bench at all.
• Functional coverage helps engineers and managers create a plan for verification which will ensure high quality and predictable schedules.

After attending this presentation you will walk away with an understanding of how and why traditional verification approaches are leaving engineers to toiling in the lab and making excuses to customers. Join Stefan Bauer, one of Mentor's verification experts, on this exciting journey to streamline your FPGA verification approaches!
Event: Stockholm, Copenhagen
Stefan Bauer, <stefan_bauer@mentor.com>, Mentor - A Siemens Business Company

Essential tools for FPGA board bring up

Abstract : As FPGAs have become the heart of an embedded system the tools needed to speedily bring a board up and allow easy debug have had to evolve. This presentation will highlight the tools and techniques available from Intel to help speed you through basic board bring-up and debug – getting your system out the door soonest!
Event: Stockholm, Copenhagen
Nikolay Rognlien - Arrow Norway AS

Winbond Flash and DRAM for the Industrial Market

Winbond's Memory solutions support FPGA based applications. This session is to introduce the portfolio and how Winbond is connected to the industry. Winbond supports Distribution initiatives such as the Arrow MAX1000 Maker Board, which will be also looked at in more detail.

Presenter: Christian Bangert, Distribution Consultant to Winbond Electronics Corporation

Data Security in IoT applications with Winbond's Authentification Flash Devices.

Security Matters in particular when it comes to Data transfer/exchange. Winbond's Athentification Flash devices address this challenge with a simple and cost effective solution to adding multi-layered authenticity to the system in all areas of an IoT system, from Host thru gateways into the cloud and apps.

Presenter: Christian Bangert, Distribution Consultant to Winbond Electronics Corporation

Contribution D – Industrial and academic tutorials

VUnit 3 - Develop Code with Confidence and Speed (90 min)

Time: 10:30 – 12:00
Room: Älgen

Please contact tutorial@synective.se **for compulsory registration (max 12 persons) and also registration on the FPGAworld.**

VUnit (vunit.github.io) is an open source testing framework for VHDL and SystemVerilog founded in 2014 by Lars Asplund from Synective Labs and Olof Kraigher from Veoneer. It features the functionality needed to realize continuous and fully automated testing of your HDL code.

VUnit doesn't replace but rather complements traditional testing methodologies by reducing test overhead. Tests can be run earlier and more frequent and bugs can be found before they become costly. VUnit improves the speed of development by supporting incremental compilation and by enabling large test benches to be split up into smaller tests executed in parallel. It increases the quality of projects by enabling large regression suites to be run on a continuous integration server.

VUnit does not impose any specific verification methodology on its users. The benefits of VUnit can be enjoyed when writing tests first or last, when writing long-running top-level tests or short and fast unit tests, when using directed or constrained random testing. VUnit also includes libraries for supporting common verification tasks.

VUnit is used by both FPGA and ASIC teams, from US to Japan, when developing everything from high-volume products like automotive vision to niche military systems, by tool providers, in research and education.

In this tutorial you will learn how you can get started by adopting your existing test benches in a few small steps. We will explore the everyday tasks performed by a VUnit user: adding test cases, running full or partial test suites, multi-core test execution, debugging failing test cases etc. You will also get acquainted with the support libraries provided by VUnit, for example logging, checking, advanced test bench communication, and bus functional models.

Flyover Cabling Solutions for High Performance Interconnect for FPGAs

Time: 13:45-14:45
Room: Älgen

Please contact Kevin.Burt@samtec.com **for compulsory registration (max 12 persons) and also registration on the FPGAworld.**

As FPGA speeds increase to 56/112 Gbps PAM4, and the number of transceivers increase, so do the system design challenges. Signal integrity, thermal and packaging considerations place extreme constraints on the entire path out of the FPGA.

Traditional PCB routings are limited by the material resulting in shorter traces or more expensive exotic materials and layout challenges getting all the 56/112 G signals routed. As a result, the Interconnect Industry has created flyover cable solutions to enable these high bandwidth, high density links. These flyover solutions enable improved Signal integrity, low system power, and high performance, high density FPGA connections by taking the high speed signals off board and into low loss cables.

In this tutorial, you will learn the challenges of using traditional PCB layout techniques as well as the advantages of copper and optical cables as well as the system advantages that they enable."

Contribution D – Industrial and academic tutorials (1,5-3 hours, Stockholm)

VUnit 3 - Develop Code with Confidence and Speed

Time: 10:30 – 12:00

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