08:30	**FPGAworld 2017** **Registration Sep 21th, DTU (SCION), Building 372, Diplomvej 2800 Lyngby**
Sponsors:	
09:00	**Conference opening** Professor Lars Dittmann, Technical University of Denmark and Lennart Lindh, FPGAworld Program Proceedings
09:15-10:00	**Keynote speaker: Hans Holten-Lund, Prevas AB** **Acceleration of Convolutional Neural Networks in FPGAs** **Abstract:** The keynote presentation will discuss some of the issues we face as FPGA designers when tasked with the computational loads involved in signal processing. New tools are appearing, aiming at making it easier to design signal processing blocks. Convolutional Neural Networks share many techniques with more traditional signal processing. Explore tradeoffs, design-time vs performance. Floating-point vs fixed-point math. GPUs vs FPGAs. **Hans Holten-Lund** is a Senior FPGA Designer at Prevas, and has a Ph.D. and M.Sc. EE from IMM, Technical University of Denmark. He has worked mainly on FPGA design for phased array ultrasound scanners, and and other embedded FPGA based systems, including computer vision. Also has industry experience with multi-gigabit networks and 3D computer graphics. A longer CV is available here: https://www.linkedin.com/in/hans-holten-lund-a3a53114/ Power Points (pdf) Session Chair: Professor Lars Dittmann, Technical University of Denmark
10:00-10:30	**Coffee Break & Exhibition**
10:30-12:00	Product Program, C1-3 Session Chair: Lennart Lindh C1: **Mastering Clock Domain Crossing challenges in FPGA Design** Stefan Bauer, Netherlands, InnoFour, More information C2: **The FPGA security challenge: high assurance on low cost devices** Thomas Ginell, Linear Technology now part of Analog Devices C3: **Intel High Level Synthesis** Nikolay Rognlien, Arrow
12:00-13:00	**Lunch Break & Exhibition**

13:00-13:30	**Mike Dini talk,** Dini Group, USA **FPGA events during the year that has gone and gossips** Session Chair: Lennart Lindh
13:30-14:30	Industrial and Student/Hackers Program, A1-3 Session Chair: Lennart Lindh A: **Constrained Random and Functional Coverage for VHDL testbenches – controlled in a structured manner** Espen Tallaksen, Norway A: **Portable Stimulus Specification - The Next Big Wave in Functional Verification** Staffan Berg, Sweden More information
14:30-15:00	**Coffee Break & Exhibition**
15:00-16:00	Industrial and Student/Hackers Program, Program, A4-6 Session Chair: Lennart Lindh **Product Presentation:** **C: Use of FPGA in high speed networking** Henrik M. Lilja, Silicom Ltd **Industrial presentation:** A: **The Impact of Place and Route on FPGA Logic Synthesis** Pieter J. Hazewindus, USA
16:00-about 16:30	Discussions **What for skills & knowledge do a FPGA designers need today?** Session Moderator: **Rolf Sylvester-Hvid**, Aktuel Elektronik, (Danish Magazine)

Exhibitors and Product Presenters Copenhagen and Stockholm	ÅF, Sweden DTU, Technical University of Denmark Aktuel Elektronik, Denmark Elektroniktidningen, Sweden Prevas, Sweden XILINX, USA	Linear Technology, USA Dini Group, USA Innofour, Netherlands Avnet Silica, Denmark Avnet Silica, Sweden Synective Labs	Silicom, Denmark Arrow, Europe SAMTEC, USA Motion Control, Sweden AGSTU Education, Sweden Analog Devices, USA Elmatica, Norway

Welcome to next FPGAworld Conference 2018
Stockholm 18 September and Copenhagen 20 September