

08:30	<p style="text-align: center;">FPGAworld 2017 (Working copy) Registration Sep 21th, DTU (SCION), Building 372, Diplomvej 2800 Lyngby</p>
<p style="text-align: center;">Sponsors:     </p>	
09:00	<p style="text-align: center;">Conference opening Professor Lars Dittmann, Technical University of Denmark and Lennart Lindh, FPGAworld</p>
09:15	<p style="text-align: center;">Keynote speaker: Hans Holten-Lund, Prevas AB</p> <p style="text-align: center;">Acceleration of Convolutional Neural Networks in FPGAs</p> <p>Abstract: The keynote presentation will discuss some of the issues we face as FPGA designers when tasked with the computational loads involved in signal processing. New tools are appearing, aiming at making it easier to design signal processing blocks. Convolutional Neural Networks share many techniques with more traditional signal processing. Explore tradeoffs, design-time vs performance. Floating-point vs fixed-point math. GPUs vs FPGAs.</p> <p>Hans Holten-Lund is a Senior FPGA Designer at Prevas, and has a Ph.D. and M.Sc. EE from IMM, Technical University of Denmark. He has worked mainly on FPGA design for phased array ultrasound scanners, and other embedded FPGA based systems, including computer vision. Also has industry experience with multi-gigabit networks and 3D computer graphics. A longer CV is available here: https://www.linkedin.com/in/hans-holten-lund-a3a53114/</p> <p style="text-align: center;">Session Chair: Professor Lars Dittmann, Technical University of Denmark</p>
10:00	<p style="text-align: center;">Coffee&Tea Break</p>
10:30 – 12:00	<p style="text-align: center;">Product Program, C1-3 Session Chair: ?</p> <p>C1: Mastering Clock Domain Crossing challenges in FPGA Design Stefan Bauer, Netherlands, InnoFour, More information</p> <p>C2: “Booked” Linear Technology, More to come!</p> <p>C3: “Booked” Arrow, More to come!</p>
12:00	<p style="text-align: center;">Lunch Break & Exhibition</p>
13:00 – 13:30	<p style="text-align: center;">Mike Dini, Dini Group, USA More to come!</p>
13:30 – 14:30	<p style="text-align: center;">Industrial and Student/Hackers Program, A1-3 Session Chair: ?</p>

	<p>A1: Constrained Random and Functional Coverage for VHDL testbenches – controlled in a structured manner Espen Tallaksen, Norway</p> <p>A2: The Impact of Place and Route on FPGA Logic Synthesis Pieter J. Hazewindus, US</p>		
14:30	Coffee Break		
15:00 – 16:00	<p style="text-align: center;">Industrial and Student/Hackers Program, Program, A4-6 Session Chair: ?</p> <p>Student projects: A4: Breakout Game with DE1-SOC board (15 min) Navid Kheradmand, Sweden Presentation, Design report</p> <p>A5: Free</p> <p>A6: Free (15 min)</p>		
16:00 – about 16:30	Panel Discussion Topic: ? Panel: ? (If you are interested, please let me know, Lennart Lindh) Session Moderator: Rolf Sylvester-Hvid , Aktuel Elektronik, (Danish Magazine)		
Exhibitors and Product Presenters Copenhagen and Stockholm	ÄF, Sweden DTU, Technical University of Denmark Aktuel Elektronik, Denmark Elektroniktidningen, Sweden Prevas, Sweden XILINX, USA	Linear Technology, USA Dini Group, USA Innofour, Netherlands Terasic, Taiwan Avnet Silica, Denmark Avnet Silica, Sweden Synective Labs	Arrow, Europe Motion Control, Sweden AGSTU education, Sweden