08:30	**FPGAworld 2016** **Stockholm, Sep 13th, Frösundaleden 2A, 169 70 Solna, SWEDEN.**		
Sponsors:   			
09:00	**Conference Opening** Thony Johansson, ÅF and Lennart Lindh, FPGAworld Room: Renen		
09:15 – 10:00	Keynote Speach, Room: Renen **The Impact of Semiconductor Trends on future FPGA platforms** Frank Förster, Intel PSG *More_information*		
10:00	**Coffee Break & Exhibition**		
10:30 - 12:00	Industrial/Student Program, Room: Renen Session Chair: TBA A1: Verifying corner cases in a structured manner - using VHDL Verification Components (VVC) *More information* A2: Physics of Failure and rational approach for Design for Reliability A3: Logging using the Altera System Console debug tool	Product Program Room: Gasellen Session Chair: TBA B1: Stratix10 - A Giant Leap in Performance and Integration B2: Xilinx Zynq® MPSoC UltraScale+™ Technical Overview B3: Low power, cost effective Imaging and Video solutions in Microsemi FPGAs	Product/Student Program Room: Räven Session Chair: TBA C1: The FPGA on a Printed Circuit Board C2: Shorten fpga development time by automate register generation and access C3: Method for IP development
12:00	**Lunch Break & Exhibition**		
	Industrial Program, Room: Renen Session Chair: TBA	Product/Student Program, Room: Gasellen Session Chair: TBA	
13:00 - 14:00	A4: Xilinx FPGAs uses a 2.5D package technology, why? *More information* A5: mm Wave radar saves lives at railway crossings - Embedded RF/FPGA development success story	B4: Automatic Formal Checks for FPGA designs B5: Increasing Performance and Predictability of a Real-Time Kernel Using Hardware Acceleration	
14:00	**Coffee Break & Exhibition**		
14:30 – 15:30	A6: FPGAs in Machine Learning applications A7: FPGA SoC for Machine Learning	B6: Power management (60 min)	
15:30	**Short Break & Exhibition**		
15:45 - 16:30	Keynote speech, Room: Renen FPGAs -- A Report from the Trenches Mike Dini		
16:30	**Go Home Drink in the Exhibition hall**		

Exhibitors	ÅF, Elektroniktidningen, MotionControl, AGSTU, Linear Technology, Arrow, Avnet, Innofour, Dini Group, ProgBit, Synective Labs, Future Electronics

Keynote Speakers 2016 Stockholm

The Impact of Semiconductor Trends on future FPGA platforms

Frank Förster, VP EMEA, Intel PSG.

Abstract: This talk will first discuss semiconductor industry trends, then it will outline the profound implication the trends will have on future FPGA platforms across multiple vertical segments.

Frank Förster is with Intel Programmable Solutions Group (formerly Altera) since 2007 in several positions. Prior to Altera, Frank Förster was working for companies in the field of Industrial Automation, Automotive as well as Digital Signal Processing. Frank Förster holds an engineering degree in EE/telecommunication.

FPGAs -- A Report from the Trenches

Abstract: Mike Dini, an old FPGA veteran, will present his view of the present state of the FPGA industry. He will address the past, present, and future of the FPGA world.

Mike Dini is the founder and president of DINI Group, a San Diego based company that specializes in the use and application of FPGAs. He has 30+ years of experience with programmable logic. Mike has a BSEE and MSEE from UCI.

Abstracts

A1 - Verifying corner cases in a structured manner - using VHDL Verification Components (VVC)

UVVM provides overview, readability, maintainability and reuse for medium to high complexity VHDL testbenches. Key enablers are a structured architecture, an easily readable test sequencer and fast VVC development. This presentation will explain the concept, show how easy value and cycle related corner cases can be targeted, and how constrained random, coverage and efficient debugging is supported.
UVVM is a true game changer with great feedback from the VHDL community, - and gaining momentum.
Espen Tallaksen, Bitvis

A2 - Physics of Failure and rational approach for Design for Reliability

Things break and the knowledge about when and how often this happen over the life time of an Electronic system (PCB) is of high value.
In this presentation we will explain the basic of Physics of Failure and how it is used for rational design for reliability.
Yehoshua Shoshan, Innofour

A3 - Logging using the Altera System Console debug tool

To enable logging for the Altera development board DE2-115 a LOGGER IP component was developed that writes event information to RAM.
The logged information is extracted using the Altera System Console debug tool. Information is parsed and saved on the host computer's file system.
The system is demonstrated using a hardware accelerated FreeRTOS RTK.
Per Östberg, AGSTU School

A4 - Xilinx FPGAs uses a 2.5D package technology, why?

Stacking one level of active dies on top of a passive die is called a 2.5D solution. A traditional SoC (System on Chip) is implemented on a single die, and placed in a package as a 2D solution.
The Xilinx FPGA Virtex-7 2000T is created as a 2.5D solution. This presentation will explain how this implementation looks like and why this 2.5D implementation outperforms, both technically and cost wise, a traditional 2D solution.
Kim Petersen, HDC

A5 - mm Wave radar saves lives at railway crossings - Embedded RF/FPGA development success story

Automobile accidents are currently killing 1.25 million people per year worldwide and soon it will reach 2 million people per year. A chilling statistic. The new mantra is “avoiding collisions.”
Qamcom 77 GHz short range Radar - Obstacle Detector System – have been improving safety for unsupervised railway crossings, but the radar is scalable for collision avoidance on moving cars/trucks, and ongoing development will make the platform capable to be used as sensor system for autonomous vehicles, upgraded to 79 GHz.
The successful 77 GHz radar uses FPGA for high speed A/D sample preprocessing, cooperation with a powerful SOC with DSP functionality. The FPGA solution is very capable for the preprocessing and SRIO protocol conversion, but with the 79 GHz enhancement the sample rate will multiply 10 times.
The 79 Ghz radar will need to move the signal processing algorithms and radar control towards the FPGA domain, and the scalable SW Defined development environment for FPGAs offers a software-centric, system-optimizing compiler that accepts existing system-level design in C or C++ and generates both the software application and the hardware configuration needed to implement the enhanced system.
The new FPGA tools employs software compilers, HLS (high-level synthesis), and prebuilt hardware infrastructure to assemble such systems.
Tryggve Mathiesen, Qamcom

A6 - FPGAs in Machine Learning applications

Machine learning is one of the fastest growing application models, and crosses every vertical market from the data center, to embedded vision applications in the IoT space, to medical and industrial applications. This presentation introduces the high-level concept of machine learning, focusing on Convolutional Neural Networks. It also explains the benefits of using an FPGA in these applications.

Nikolay Rognlien, Arrow

A7 - FPGA SoC for Machine Learning

Machine Learning is on the verge of creating a technology revolution. The capability to learn and analyse differentiates the next-generation machines from the current ones. The machine learning algorithms which exist today mostly run on high-end processors and GPUs. These algorithms need optimization of both power and performance to meet the stringent requirements of real-time embedded systems. This presentation describes why FPGA SoC is a good fit for such applications and what more the FPGA vendors can do to make it a better fit.

Shaji NM, QuEST Global Engineering Services Pvt. Ltd., Trivandrum

B1 - Stratix10 - A Giant Leap in Performance and Integration

Learn more about Altera's groundbreaking new Stratix® 10 device family and how it's architecture delivers extreme performance, many transceiver options and integration of high bandwidth DRAM into one device package.

Nikolay Rognlien, Arrow

B2 - Xilinx Zynq® MPSoC UltraScale+™ Technical Overview

· The new MPSoC Processing System Architecture
· UltraScale+ Fabric (PL) Architecture
· Development Software and tools
· Development boards and Availability

Per Boström, Avnet

B3 - Low power, cost effective Imaging and Video solutions in Microsemi FPGAs

The adaptable nature of FPGAs is well suited for video applications in different systems. Microsemi unique flash-based FPGAs provide a low power platform for the image sensor interface, video signal processing, video compression and display interface.

A wide range of free imaging/video IPs from Microsemi together with 3rd party IP offerings shortens development time and reduces the system cost.

Anders Hillström, Microsemi

B4 - Automatic Formal Checks for FPGA designs

RTL designers can't wait for a test bench to begin checking the quality of their code and verifying the functionality they've started to implement is on the right track. Assertion-based verification can be employed, but even basic properties in standard languages like SVA or PSL are time consuming to create, debug, and maintain.

The Questa AutoCheck app makes it easy to triage bugs that would otherwise require a lot of time and effort to eliminate, such as state-machine deadlock and livelock, arithmetic overflow, out-of-range memory indexing and many more. AutoCheck's rich debugging environment pinpoints the root cause of these bugs with schematics, waveforms and FSM state diagrams, making it quick and easy to use.

Rick Stroot, Innofour

B5 - Increasing Performance and Predictability of a Real-Time Kernel Using Hardware Acceleration

A real-time kernel offers many advantages when developing safety critical real-time applications. However, these benefits come at a price as the use of a real-time kernel can introduce both latency and non-determinism into the system. I will be presenting a hardware accelerated implementation of the widely popular real-time kernel FreeRTOS, using only off-the-shelf HW components. This HW/SW implementation was developed as part of my degree project in an attempt to increase both performance and predictability of the FreeRTOS kernel.

Jonatan Lövgren, KTH

B6 - Power management (60 min)

The latest generation of <20nm FPGAs have challenging power sequencing and voltage regulation requirements. Our presentation will explore these requirements and Linear Technology's proven solutions using Power Systems Management (PSM) products to satisfy them. We'll demonstrate how the LTpowerPlay GUI and PSM products working together accelerate your development path, validating your design and simplifying debug.

Mike Holloway, creator of LTpowerPlay GUI and Applications Engineering Manager for LTC.

C1 - The FPGA on a Printed Circuit Board

Even a FPGA needs a carrier. High pin-count IC / FPGA packages need layers of high-density interconnect (HDI) / microvias, advanced routing and stack up of the PCB.

We will look at The FPGA on a Printed Circuit Board

- Routing out from a «FPGA (BGA)» related to BGA pitch.
  - Design suggestions for BGA (0.8mm , 0.5mm and 0.4mm pitch)
- HDI Design rules
  - Materials, different HDI via-structures, «ALIVH» (Anylayer Inner Via Hole)
  - Stacked & Staggered mVias, Buried vias, Filled & Capped vias
  - Eliminate throug hole vias using existing via span, Capabilities
  - Decide IPC Class (2 or 3) before you start your layout
- Impedance requirements and considerations
- The importance of a net-list in PCB production

John Steinar Johnsen, Elmatica

C2 - Shorten fpga development time by automate register generation and access

The autoreg and autocom tools can substantially shorten fpga development time by automatically generate vhdl, c and tcl code based on a single source definition file and provide technology independent access to fpgas via simulator, jtag, ethernet(ip/udp), serial interfaces, AXI4-Lite and other processor buses. It generates synthesizable templates and communication stacks so that you can read and write to an fpga within minutes of starting a new project. A lot of effort has been gone into supporting design reuse, technology and protocol independence so that the tools can be used in many different types of projects.

The fpga developer can start by defining and accessing registers in the simulator, then move to a development board and access the fpga via the same methods. There is no need to wait for sw and hw support. When hw becomes available the fpga developer can use the board without> sw support and when sw is ready the fpga developer access the registers in parallel. This simplifies the sw/fpga integration because the fpga developer has an independent access to all registers and can see what sw does.

Every company that uses fpgas need a subset of the functionality above and many companies invest substantial time and effort into it. We've visited a lot of companies and seen the huge duplicate effort that is sunk into what is basically standard infrastructure. Our idea is to specialize into hw/fw/sw integration so that the user of our products can focus on their idea and their end product.

Arin Morten Kjempenes, ProgBit AS

C3 - Method for IP development

The project was carried out for the company Motion Control which develops electronics. Its scope is the development of a method for constructing IP components of digital filter algorithms for implementation on a FPGA . A low pass filter component was constructed and every step of the process was carefully documented. From the process a construction and verification method was derived.

Raul Alderete Miranda, AGSTU and Motion Control