

**MAX 10→**

*The Next Step In Low Cost FPGA Integration*

FPGA World

September 2015



**ALTERA**<sup>®</sup>  
MEASURABLE ADVANTAGE™

# Innovation Leader Across the Board

# ALTERA®



**FPGAs and CPLDs**

**Low Cost,  
Non-volatile**

**FPGAs**

**Cost/Power Balance  
SoC & Transceivers**

**FPGAs**

**Mid-range FPGAs  
SoC & Transceivers**

**FPGAs**

**Optimized for  
High Bandwidth**

**PowerSoCs**

**High-efficiency  
Power Management**

## RESOURCES

**Embedded Soft and  
Hard Processors**

**Nios® II  
ARM**

**Design  
Software**



QUARTUS® II

**DSP Builder**

**Development  
Kits**



**Intellectual  
Property (IP)**

- Industrial
- Computing
- Enterprise



# **GENERATION**10

*Portfolio of FPGAs and SoCs*

**TSMC 55 nm Embedded Flash**

**Instant-on, low-cost,  
non-volatile FPGAs**



**TSMC 20 nm**

**Highest Performance  
20 nm FPGA and SoCs**

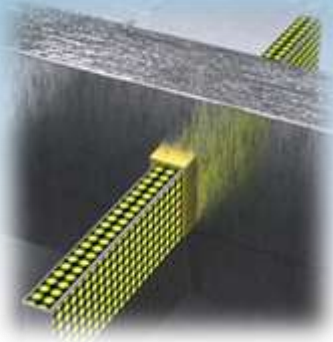


**Intel 14 nm Tri-gate**

**2x Higher Core  
Performance vs. 28 nm**



Best in class  
Semiconductor  
Innovation & Technology



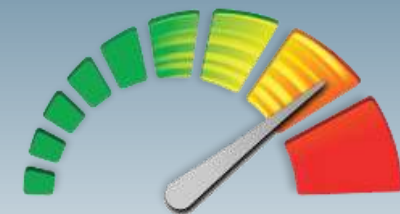
Compelling New Device  
Architectures

Industry's First FPGA with  
IEEE 754 Floating Point



**HyperFlex**<sup>™</sup>  
ARCHITECTURE

Strategic Investments  
That Open  
Up New Markets



OpenCL

*Expanding Opportunities for FPGAs*

# 2X

Core Performance

# 5.5M

Logic Elements

Up to **70%**  
Lower Power

Up to **10**  
TFLOPS

Most  
Comprehensive  
**Security**



Heterogeneous  
**3D SiP**  
Integration

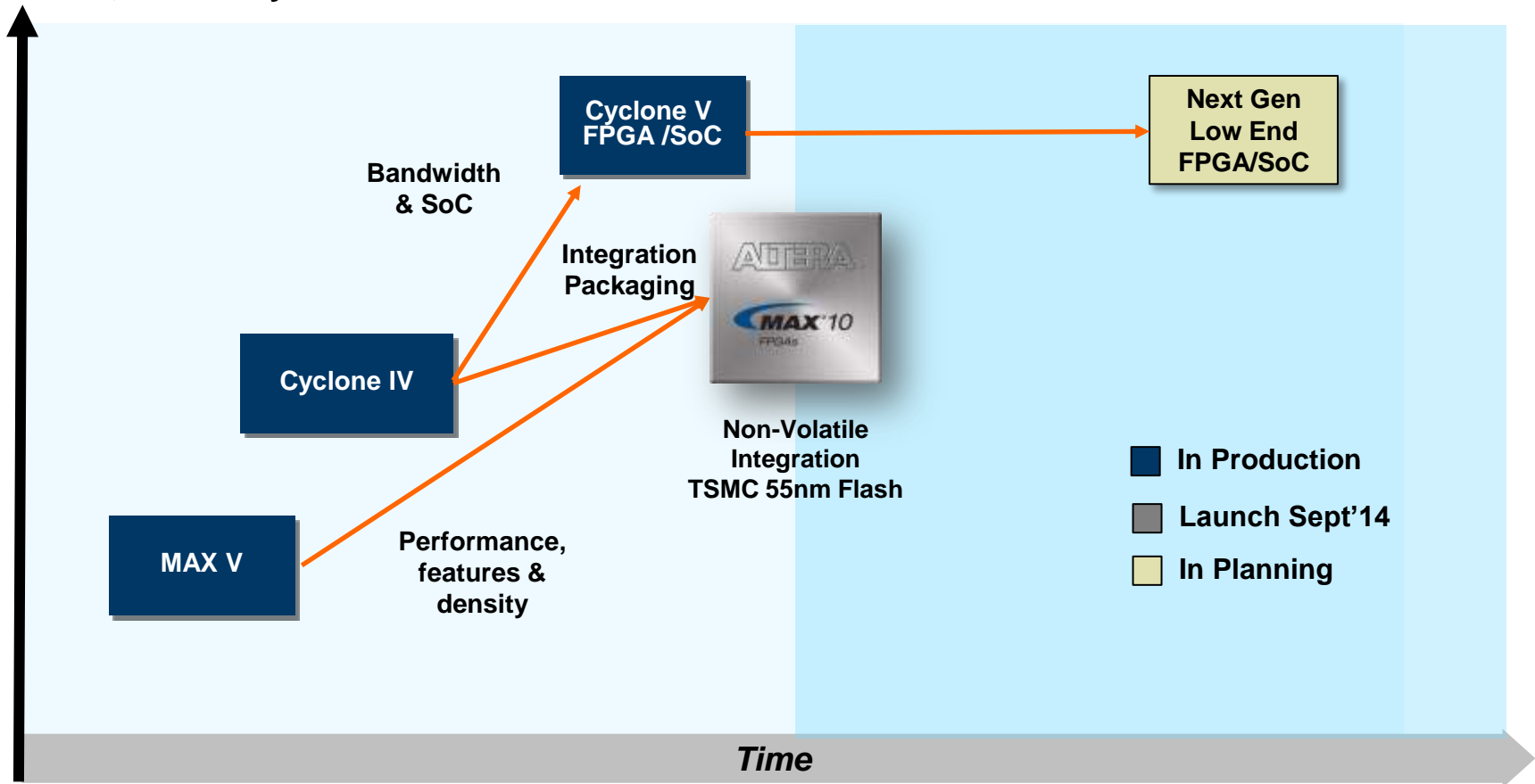
Intel **14 nm**  
Tri-Gate

Quad-Core  
**Cortex-A53**  
ARM Processor

# ALTERA®

# Altera Continues Focus & Investment in Low End Families

More performance,  
features, or density



## What makes it different ?

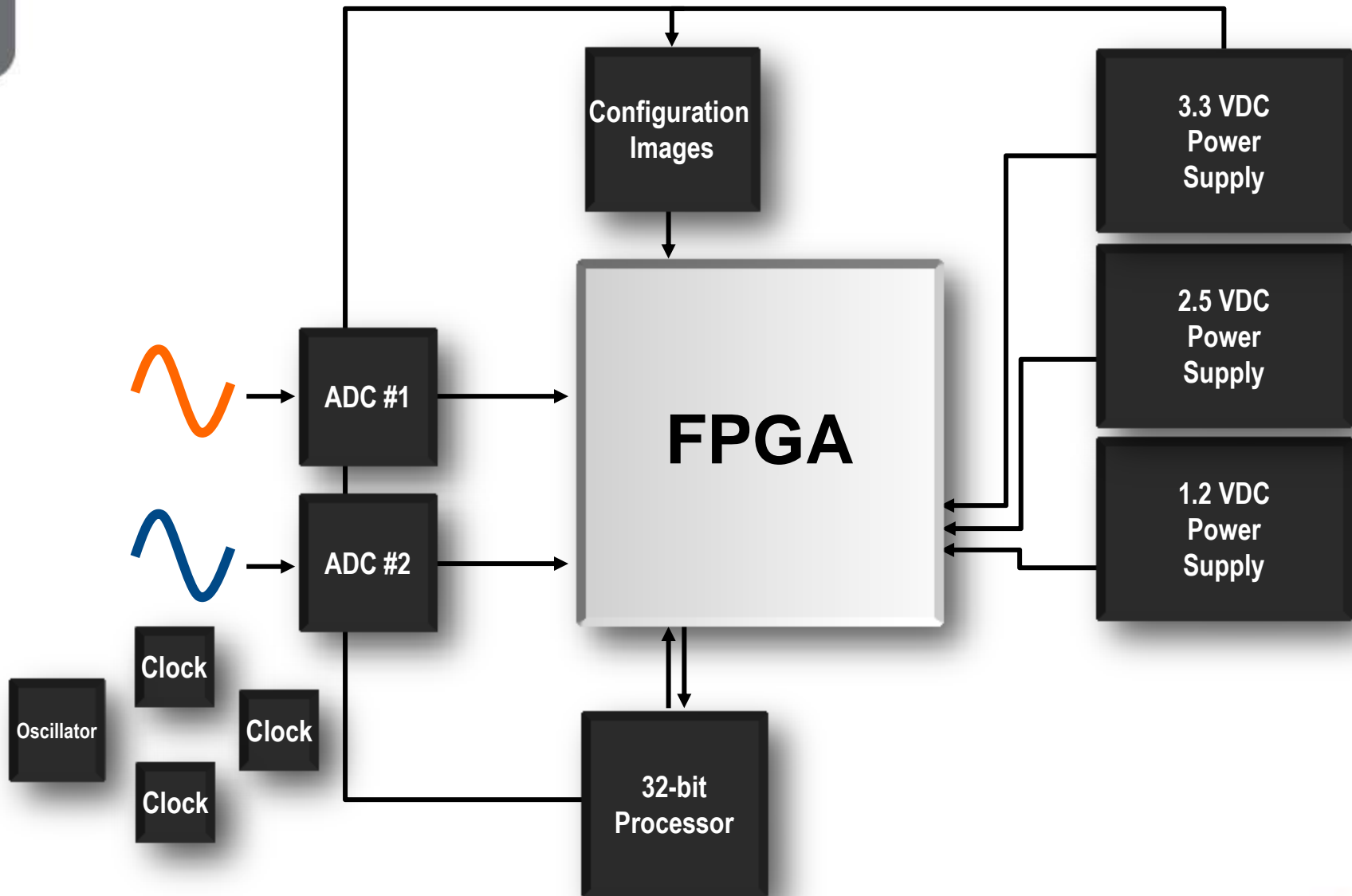
- ◀ Dual Non Volatile Images
  - Internal Flash to hold two images
  - Faster time to operation
- ◀ Secure Configuration
  - Two stage boot feature, AES
- ◀ Integrated ADC
  - Flexible sampling
- ◀ Soft Processor Support
  - Secure Internal Boot
- ◀ Single Supply

It's time to rethink  
what an FPGA is.

[altera.com/max10](http://altera.com/max10)



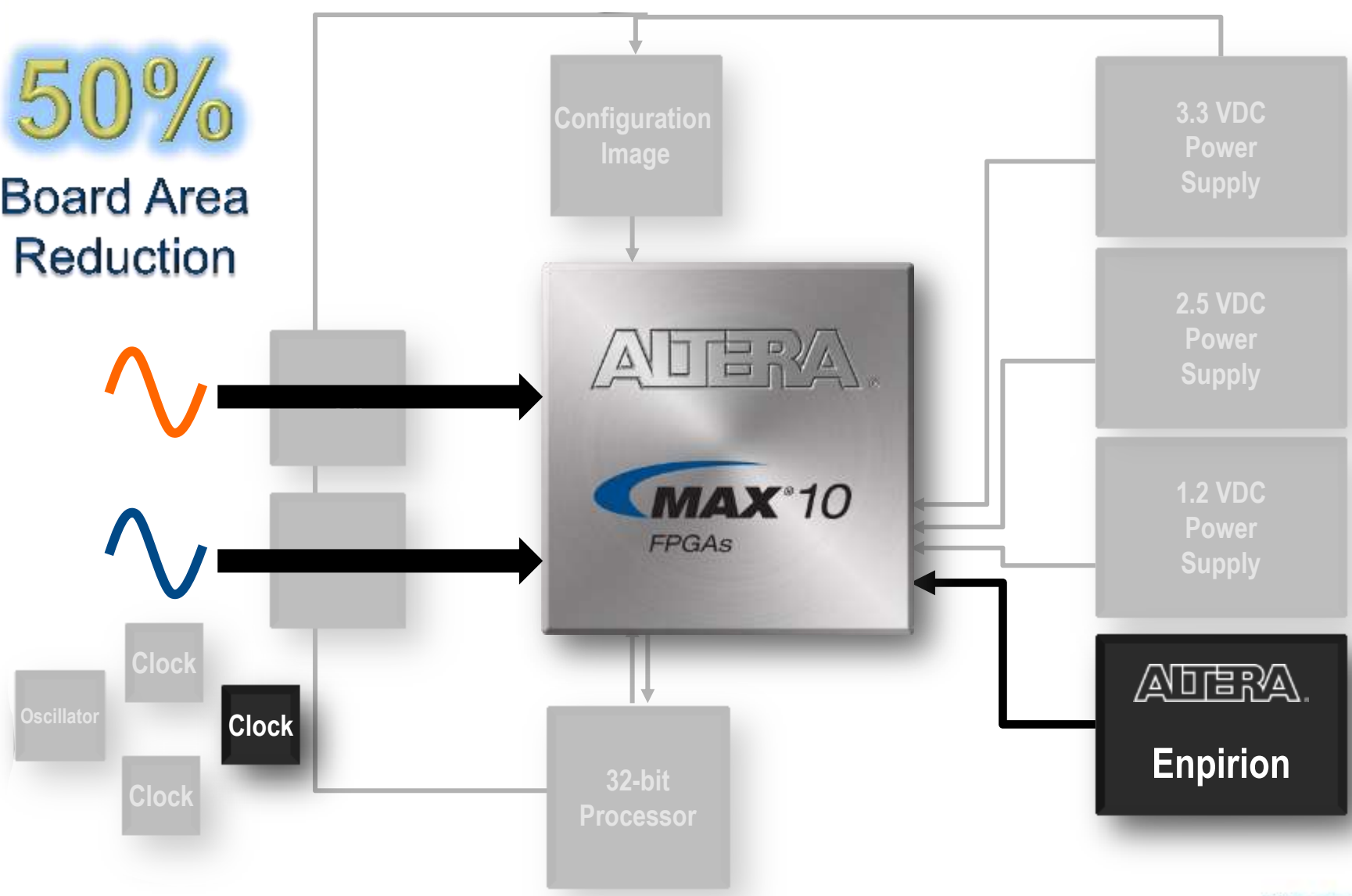
# Traditional FPGA System Components





# MAX 10 Simplifies Traditional FPGA Systems

**50%**  
Board Area  
Reduction



# Lower BOM, Smaller PCB Area, Instant-on Configuration

Up to 50K Logic Elements

Packages as small as 3 x 3 mm



## Flash Memory (NOR)

- User Flash
- Configuration Flash 1
- Configuration Flash 2

12-bit SAR ADCs

Power Regulator

4 PLLs

8 I/O Banks

DSP Blocks

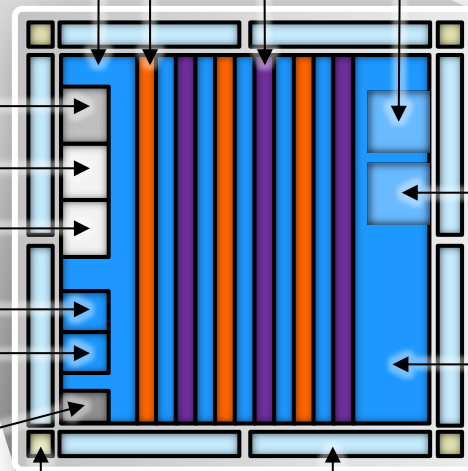
RAM Blocks

DDR3 Controller

# Nios<sup>®</sup> II

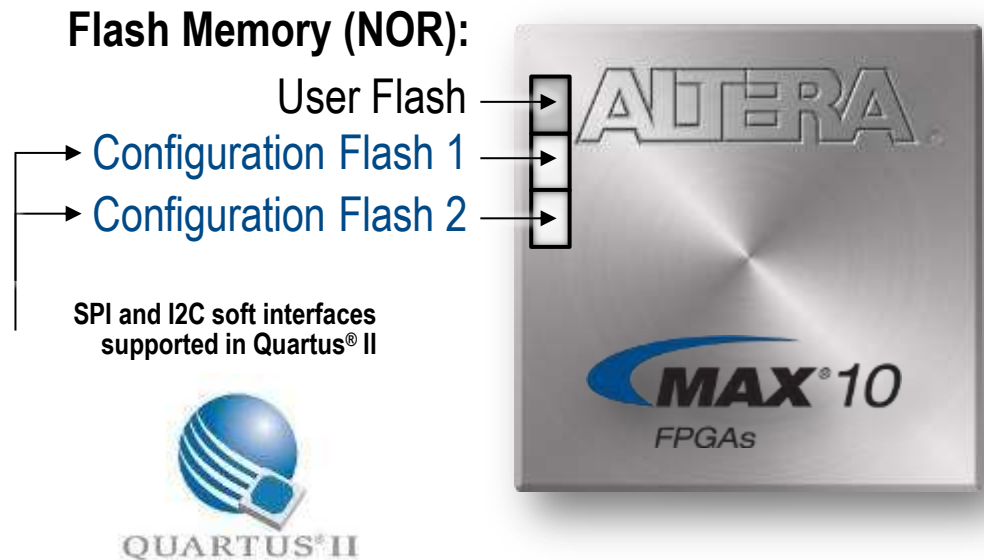
32-bit Processor

On-chip Oscillator



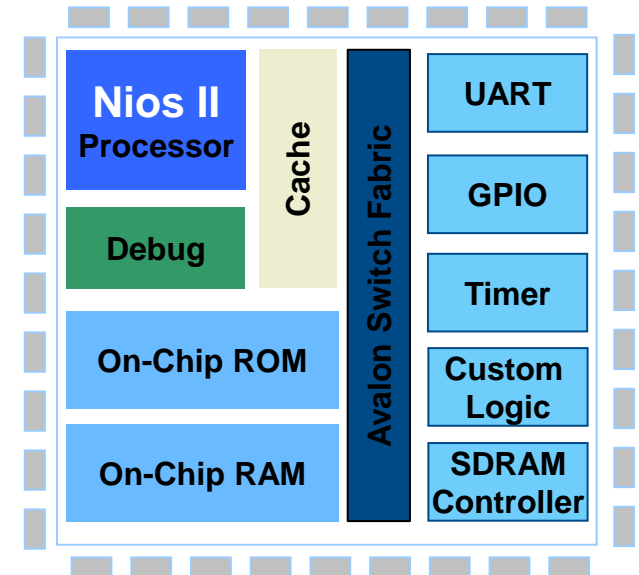
# Integrated Embedded Flash Increases System Value

- Lower total cost of ownership
  - Reduced BOM
  - Smaller board area
- Reduced system risk
  - Fewer vendors to manage
  - Simpler PCB design
  - Supports long life cycles
- Fail-safe remote updates
  - Store two configuration images
- Improved system management
  - Instant-on configuration
  - Power-up sequencing



# Embedded Processing Capabilities Increase System Value

- Single-chip embedded processor system
  - Soft core Nios II processor support
  - Very small footprint
  - No external RAM or storage needed
- User-customizable processor
  - Flexibility MCUs don't offer
- Supports real-time applications
  - Configuration in under 10 ms
  - Meets automotive and industrial regulatory requirements
- Supports longer life cycles



Customizable logic

## Nios<sup>®</sup> II

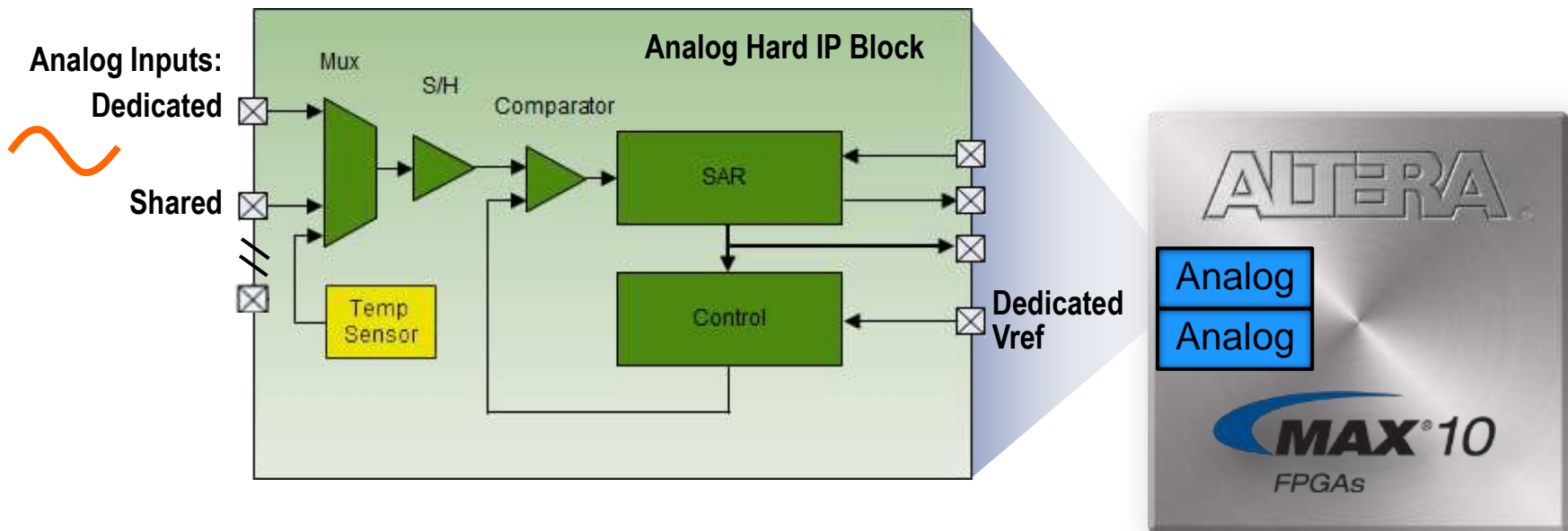
# Increase System Value with Integrated Analog Blocks

## ◀ In-chip system monitoring

- Integrated ADCs
- Reduce board space
- Flexible sample sequencing
- Lower latency

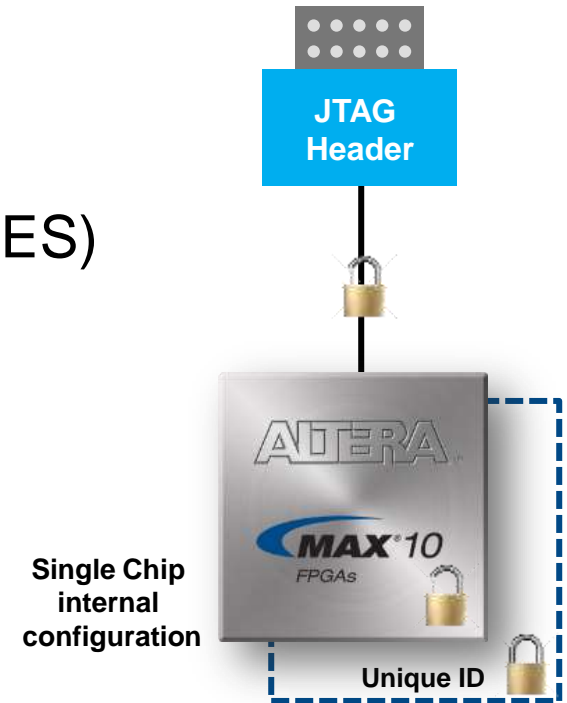
## ◀ Measure environmental conditions

- Integrated temperature sensor



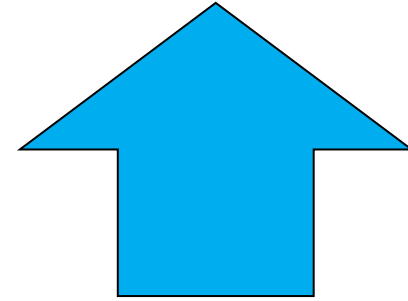
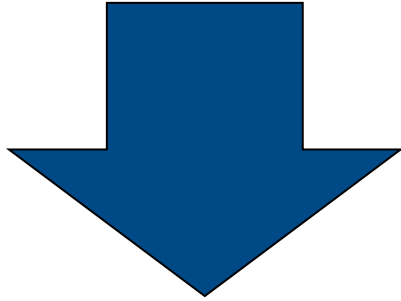
# Increase Security by adding Anti Tamper Features

- Single chip solution with up to 2 secure images
- Advanced Encryption Standard (128-bit AES) protection
  - Non-volatile key for external & internal configuration
- JTAG port security protection
  - Read disable or Read/Write disable (OTP)
  - Prevents reverse engineering
- Chip ID
  - Non volatile 64 bit unique ID for asset traceability
- Verify Protect
  - Allows disabling of CFM read back



# MAX 10 FPGA Customer Benefits

## Lowers System Cost

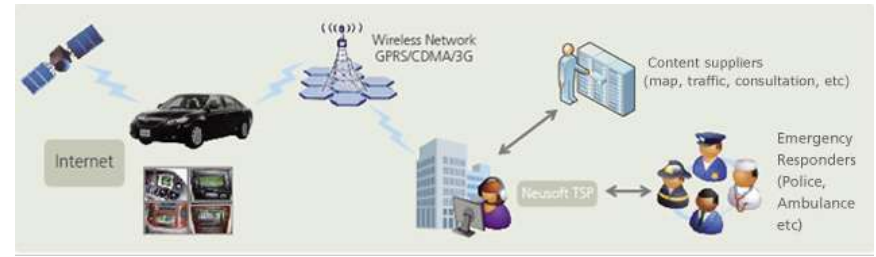


## Increase Board Reliability

Single-chip integration item	Customer Benefits
N-components → 1 component	Higher system reliability (less failure points) Reduced BOM/System Cost
Reduced PCB Footprint	Simpler PCB Design Fewer PCB layers → Lower PCB cost
Fewer Suppliers	Less vendors to manage
PLD have Longer Life-cycles	Avoids EOL vs. other technologies

# So where does it fit ?

➤ No right or wrong answer



Consumer



Motor Driving



Automotive - Infotainment



Commercial



Secure Applications



Industrial – Factory Automation



Machine Vision



## MAX 10 FPGA – Family Plan

Device	LEs	Block Memory (Kbits)	18x18 Mults	PLLs	Internal Config.	User Flash <sup>1</sup> (KBytes)	ADC, TSD	External RAM I/F
<b>10M02</b>	2,000	108	16	1, 2	Single	12	-	Yes <sup>2</sup>
<b>10M04</b>	4,000	189	20	1, 2	Dual	16 – 156	1, 1	Yes <sup>2</sup>
<b>10M08</b>	8,000	378	24	1, 2	Dual	32 – 172	1, 1	Yes <sup>2</sup>
<b>10M16</b>	16,000	549	45	1, 4	Dual	32 – 296	1, 1	Yes <sup>3</sup>
<b>10M25</b>	25,000	675	55	1, 4	Dual	32 – 400	2, 1	Yes <sup>3</sup>
<b>10M40</b>	40,000	1,260	125	1, 4	Dual	64 – 736	2, 1	Yes <sup>3</sup>
<b>10M50</b>	50,000	1,638	144	1, 4	Dual	64 – 736	2, 1	Yes <sup>3</sup>

**Notes:**

1. User Flash depends upon configuration option.
2. SRAM only.
3. SDR SDRAM, SRAM, DDR3, DDR2, or LPDDR2.
4. ADC blocks available on die but may not be available in low pin count packages.

# Development Tools and Solutions



# Quartus II Software and IP Support

## ◀ Quartus® II software

- Number one design software in performance and productivity
- MAX 10 FPGA compilation & EPE support
  - ◀ Flash and ADC Megawizards (New!)
  - ◀ Analog Tool Kits for ADC evaluation and debug (New!)

## ◀ Includes Qsys system integration and DSP Builder for increased productivity

- Nios II support and DSP Builder + Advanced Block-set

## ◀ Abundant IP & reference designs

- [Altera Design Store](#) (New!)



***Quartus II Web Edition Software  
Complete MAX 10 support at no Cost!***

# MAX10 FPGAs App Notes & Design Examples

## Available on Design Store

AN 496 - Using the Internal Oscillator in Altera MAX Series

AN 547: Putting Altera MAX Series in Hibernation Mode Using User Flash Memory

AN 425: Using the Command-Line Jam STAPL Solution for Device Programming

AN 502: Implementing an SMBus Controller in Altera MAX Series

AN 630: Real-time ISP and ISP Clamp for Altera MAX Series

AN 494: GPIO Pin Expansion using I2C Bus Interface in Altera MAX Series

AN 485: Serial Peripheral Interface Master in Altera MAX Series

AN 486: SPI to I2C Using Altera MAX Series

AN 488 - Stepper Motor Controller using Altera MAX Series

AN 294: Crosspoint Switch Matrices in Altera MAX Series

AN 501: Pulse Width Modulations Using Altera MAX Series

AN 500: NAND Flash Memory Interface with Altera MAX Series

AN 509: Multiplexing SDIO Devices Using Altera MAX Series

AN 490: Altera MAX Series as Voltage Level Shifters

AN 265: Using Altera MAX Series as a Microcontroller I/O Expander

AN 286: Implementing LED Drivers in Altera MAX Series

AN 498: LED Blink Using Power Sequencing in Altera MAX Series

AN 495: IDE/ATA Controller Using Altera MAX Series

AN 492: CF+ Interface using Altera MAX Series

AN 493: I2C Battery Gauge Interface using Altera MAX Series

AN 491: Power Sequence Auto-start Using Altera MAX Series

# MAX 10 Designs in the Design Store

Long list of MAX 10 designs - tested, packaged, and ready to use with Quartus

The screenshot shows the Altera Design Store interface. At the top, there's the Altera logo and a 'Login' button. Below that, the 'Design Store' header is visible. A navigation bar includes 'Development Kits' and 'Design Examples'. A search bar is present with filters for 'Family' (MAX 10), 'Quartus II Version' (Any), and 'Vendor' (Any). The main content area displays a list of design examples with columns for Name, Category, Board, Family, Device, Version, Quartus II Version, and Vendor.

Name	Category	Board	Family	Device	Version	Quartus II Version	Vendor
Defining MAX 10 in Baseline Design	Design Example	BeMicro MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
CompactFlash+ Interface (AN 482)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Crosspoint Switch Interfaces in MAX devices (AN 234 - custom example)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Crosspoint Switch Interfaces in MAX devices (AN 234 - switch example)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Dashboard Design Example	Design Example	MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Dashboard Design Example-Deflino	Design Example	BeMicro MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
DPD Pin Expansion Using DC Bus Interface (AN 484)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
DC Battery Gauge Interface (AN 490)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.01	14.0.2	Altera
DEDATA Controller (AN 488)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Implementing an SMBus Controller (AN 502)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Implementing LED Drivers in MAX devices (AN 290)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera

LED Blink Using Power Sequencing (AN 486)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
MAX 10 Evaluation Kit Baseline Design	Design Example	MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Microcontroller I/O Expansion (AN 291)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Multiplexing SIO Devices (AN 500)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
NAND Flash Memory Interface (AN 503)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
On-chip Temperature Sensor Design Example	Design Example	MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Power Sequence Add State (AN 481)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Pulse Width Modulation (AN 487)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Running Altera's Bus Series in Hierarchical using User Flash Memory (AN507)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
PWM Design	Design Example	MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Restore Factory Settings (LED Flash)	Design Example	MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Serial Peripheral Interface Master (AN 485)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	0.9	14.0.2	Altera
Simple PWM Design	Design Example	BeMicro MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	0.9	14.0.2	Altera
Stepper Motor Controller (AN 483)-BeMicro	Design Example	BeMicro MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Stepper Motor Controller (AN 483)	Design Example	MAX 10 FPGA Evaluation Kit	MAX 10	10M10SDA	1.0	14.0.2	Altera
Using the Internal Oscillator in MAX devices (AN 406)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera
Voltage Level Shifters (AN 480)	Design Example	MAX 10 Design Examples	MAX 10	10M10SC	1.0	14.0.2	Altera

Showing 1 to 26 of 26 entries

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<https://cloud.altera.com/devstore/platform>

## Altera MAX 10 Kit Demos / Design Examples

Kit Demos and Design Examples	Available	Target	Location
Sleep Mode Demo Design Dev Kit	Now	10M50 Dev Kit	Kit installed
Dual Configuration Dev Kit	Now	10M50 Dev Kit	Kit installed
Remote System Update Dev Kit	Now	10M50 Dev Kit	Design Store
Board Management Controller Reference Design	Q3'15	10M50 Dev Kit	Design Store
Nios II Golden HW Reference Design	Now	10M50 Dev Kit	Design Store
Nios II NEEK Full Featured Design	Q3'15	MAX 10 NEEK	Design Store
Nios II Ethernet Design	Now	10M50 Dev Kit	Design Store
Nios II MCU Replacement Designs	Now	--	Design Store
MAX 10 Kit Base Designs (pin assignments)	Now	All Kits	Design Store
Nios II Arduino LCD Design ( <u>Eval Kit</u> )	Now	10M08 Eval Kit	Design Store

*Base designs great, fast way to start a kit design*

# End Market BU Reference Designs

Demos and Design Examples	BU Segment	Location	Target Date*
Industrial Ethernet Multi-protocol	Industrial-Ethernet	By request	Q3
Drive-on-Chip FOC	Industrial – Motor Control	By request	Q3
DC-DC Conversion	Industrial -Motor Control	Design Store	Available Now
I/O Module Controller	Industrial – I/O	By request	Late Q2
Info: MIPI Demo	Automotive	By request	Q3
Advanced Driver Assist	Automotive	By request	Q3

# MAX<sup>®</sup> 10 FPGA Kit Portfolio



~\$29 - \$69

## **MAX 10 FPGA Evaluation Kits**

- ◀ Ultra Low Cost Eval
- ◀ Logic, I/O, power Eval
- ◀ Arduino
- ◀ 4 package/density options to choose
- ◀ Enpirion PowerSoCs



~\$199

## **MAX 10 FPGA Development Kit**

- ◀ High Density Development
- ◀ Ref Design Platform
- ◀ 300 MHz DDR3
- ◀ ADC Evaluation (SMAs)
- ◀ HDMI TX, HSMC
- ◀ Enpirion PowerSoCs



~\$359

## **Altera NEEK 10 Kit**

- ◀ CIII NEEK Evolution with applications ported
- ◀ Large multi-touch screen
- ◀ Sensors, accelerometers, wireless
- ◀ Available end of July 2015

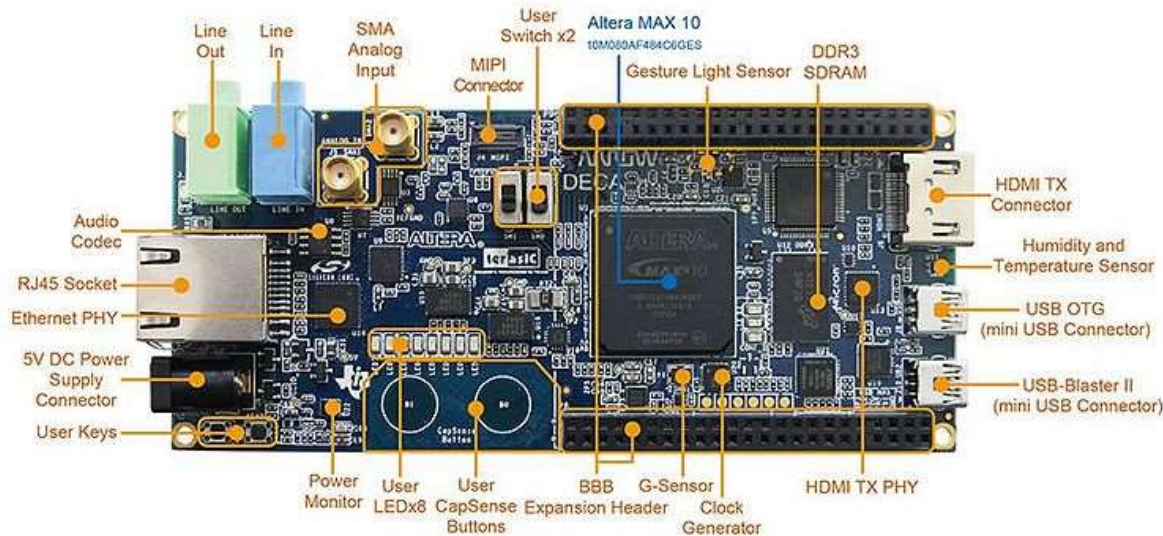
**[More Kits and Solutions in Back-Up](#)**



# Arrow DECA 10 Workshops

## Build Hands-On Experience

- Silkeborg, Arrow office, October 6th
- Herlev, Arrow office, October 7th



<http://www.arroweurope.com/news-events/events-webinars/detail/article/arrow-altera-deca-workshops.html>

# Thank You

## It's time to rethink what an FPGA is.

[altera.com/max10](http://altera.com/max10)

