ELMATICA®

FPGA world

FPGA World Conference

Stockholm 08 September 2015

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IPC-A-600
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Agenda

- IPC 4101C Materials
- Routing out from a «FPGA (BGA)» related to BGA pitch.
- Design suggestions for BGA (0.8mm , 0.5mm and 0.4mm pitch)
- HDI Design rules
- Different HDI via-structures, “ALIVH -Anylayer Inner Via Hole

  Stacked & Staggered mVias , Buried vias , Filled & Capped vias Capabilities.
- Impedance requirements and considerations
- Eliminate throug hole vias using existing via span.
- Sample on known stackups.

Materials

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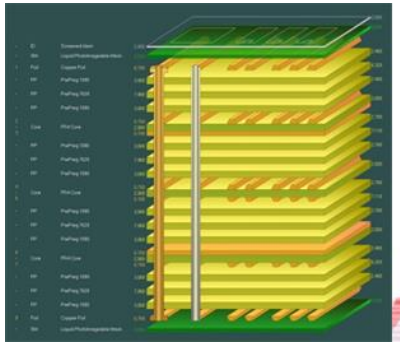
Brief introduction to IPC-4101D-WAM1

Specification for Base Materials , for Rigid and Multilayer Printed Boards



Materials

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Layer stack-up (Balanced build):

- In order to review for the balanced build, consider an imaginary line in the middle of the board. This will divide the board into **upper** and **lower** half.
- **The copper layers** in the top half of the board should match with the bottom half of the circuit board.
- **The layer to layer** spacing in the top half of the board should match with the bottom half of the board.
- **The material used** in the upper and lower half of the board should be the same to avoid warpage.
- The stack-up for hybrid circuits should be reviewed by design to design basis.

Steps in High-Speed PCB Stackup Planning

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1. Determine how many **signal layers** are needed

2. Determine how many **power planes** are needed — Distribute Power and Ground

3. **Arrange signals and planes** accordingly — Partner planes for signal layers
   — Parallel plate capacitance between Pow and Gnd — Select dielectric materials.

4. Set **signal height** above planes for **crosstalk** requirements

5. Set **trace widths** to meet **impedance** goals (Consider component I/O pitch)
   — Differential signals, in particular

6. Set **plane spacing** to meet **capacitance** requirements

7. Set spacing between signal layers to meet **overall thickness**

Materials

4 layer Standard 1.6mm foil build

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UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 5/6/2014 | Total Board Thickness: 1539 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	200	Signal	Top	Conductive			38	304.8	304.8	0.73	54.29	96.43		
		Prepreg		Dielectric	4.3	203.2								
2		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	990.6								
3		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	203.2								
4		Signal	Bottom	Conductive			38	304.8	304.8	0.73	54.29	96.43		
		Soldermask		Dielectric	3.3	12.7								

It is common to see four layer boards stacked as above. 2 layer core with 2 foil layers. That is, four evenly spaced layers with the planes in the centre. Although, this certainly makes the board symmetrical it doesn't help the EMC.

To put the power planes closer in the middle certainly creates good inter plane capacitance, but it doesn't help with signal integrity, crosstalk or EMC

Materials

6 layer Standard 1.6mm foil build

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UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 5/6/2014 | Total Board Thickness: 1564.4 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203	Signal	Top	Conductive			38	304.8	304.8	0.73	54.29	96.43		
		Prepreg		Dielectric	4.3	203.2								
2		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	355.6								
3		Signal	Inner 3	Conductive			33	304.8	304.8	0.66	56.35	92.31	67.37	
		Prepreg		Dielectric	4.3	304.8								
4		Signal	Inner 4	Conductive			33	304.8	304.8	0.66	56.35	92.31	67.37	
		Core		Dielectric	4.3	355.6								
5		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	203.2								
6		Signal	Bottom	Conductive			38	304.8	304.8	0.73	54.29	96.43		
		Soldermask		Dielectric	3.3	12.7								

A six layer board is basically a four layer board with two extra signal layers added between the planes.

This improves the EMI dramatically as it provides two buried layers for high-speed signals and two surface layers for routing low speed signals.

Materials

8 layer Standard 1.6mm foil build

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UNITS: um

Total Board Thickness: 1539.6 um

Differential Pairs > Pair 1

Layer No.	Via Span & Hole Diameter		Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
			Soldermask		Dielectric	3.3	12.7								
1	200	100	Signal	Top	Conductive			38	150	115	0.36	49.89	89.01		
			Prepreg		Dielectric	4.3	76.2								
2			Plane	GND	Conductive			33							
			Core		Dielectric	4.3	304								
3			Signal	Inner 3	Conductive			17	200	136	0.23	57.21	100.4		
			Prepreg		Dielectric	4.3	200								
4			Plane	VCC	Conductive			17							
			Core		Dielectric	4.3	203.2								
5			Plane	VDD	Conductive			17							
			Prepreg		Dielectric	4.3	200								
6			Signal	Inner 6	Conductive			17	150	180	0.28	50.32	84.96		
			Core		Dielectric	4.3	304								
7			Plane	GND	Conductive			33							
			Prepreg		Dielectric	4.3	76.2								
8			Signal	Bottom	Conductive			38	225	100	0.32	53.21	99.77		
			Soldermask		Dielectric	3.3	12.7								

Improved EMC performance, planes between each signal layer. This reduces coupling hence crosstalk dramatically. This configuration is commonly used for e.g. high speed signals of DDR2 and DDR3 designs where crosstalk due to tight routing is an issue.

Materials

10 layer Standard 1.6mm foil build

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UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 5/6/2014 | Total Board Thickness: 1579.6 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203	Signal	Top	Conductive			38	203.2	101.6	0.33	53.65	99.68		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	127								
3		Signal	Inner 3	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Prepreg		Dielectric	4.3	127								
4		Signal	Inner 4	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Core		Dielectric	4.3	127								
5		Plane	VDD	Conductive			33							
		Prepreg		Dielectric	4.3	457.2								
6		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	127								
7		Signal	Inner 7	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Prepreg		Dielectric	4.3	127								
8		Signal	Inner 8	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Core		Dielectric	4.3	127								
9		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
10		Signal												
		Soldermask		Dielectric	3.3	12.7								

A ten layer board should be used when six routing layers and four planes are required and EMC is of concern. This stackup is ideal because of the tight coupling of the signal and return planes, the shielding of the high speed signal layers, the existence of multiple ground planes, as well as a tightly coupled power/ground plane.
"Prepared for mVia use"

12 layer Standard 1.6mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 5/6/2014 | Total Board Thickness: 1554.2 um

Differential Pairs > Pair 1

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Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	200 100	Signal	Top	Conductive			38	203.2	101.6	0.33	53.65	99.68		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	127								
3		Signal	Inner 3	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Prepreg		Dielectric	4.3	127								
4		Signal	Inner 4	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Core		Dielectric	4.3	127								
5		Plane	VDD	Conductive			33							
		Prepreg		Dielectric	4.3	152.4								
6		Signal	Inner 6	Conductive			33	304.8	101.6	0.3	52.32	100.27	73	
		Core		Dielectric	4.3	127								
7		Signal	Inner 7	Conductive			33	304.8	101.6	0.3	52.32	100.27	73	
		Prepreg		Dielectric	4.3	152.4								
8		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	127								
9		Signal	Inner 9	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Prepreg		Dielectric	4.3	127								
10		Signal	Inner 10	Conductive			33	304.8	101.6	0.3	52.45	98.94	54.15	
		Core		Dielectric	4.3	127								
11		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
12		Signal	Bottom	Conductive			38	203.2	101.6	0.33	53.65	99.68		
		Soldermask		Dielectric	3.3	12.7								

The above twelve layer, 2 signal layers are added in the middle, and stackup provides shielding on six of the internal layers. “Prepared for mVia use”

The fourteen layer stackup below is used when eight routing (signal) layers are required plus special shield of critical nets is required. Layers 6 and 9 provide isolation for sensitive signals while layers 3 & 4 and 11 & 12 provide shielding for high speed signals.

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14 layer Standard 1.9mm foil build

UNITS: um | ICD STACKUP PLANNER FX – www.icd.com.au | 5/6/2014 | Total Board Thickness: 1975.8 um

Differential Pairs > Pair 1

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	203	Signal	Top	Conductive			38	203.2	101.6	0.33	53.65	99.68		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	152.4								
3		Signal	Inner 3	Conductive			33	304.8	101.6	0.3	50.26	93.74	14.24	
		Prepreg		Dielectric	4.3	76.2								
4		Signal	Inner 4	Conductive			33	304.8	101.6	0.3	50.26	93.74	14.24	
		Core		Dielectric	4.3	152.4								
5		Plane	VDD	Conductive			33							
		Prepreg		Dielectric	4.3	177.8								
6		Signal	Inner 6	Conductive			33	152.4	101.6	0.3	51.36	89.35		
		Core		Dielectric	4.3	177.8								
7		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
8		Plane	GND	Conductive			33							
		Core		Dielectric	4.3	177.8								
9		Signal	Inner 9	Conductive			33	152.4	101.6	0.3	51.36	89.35		
		Prepreg		Dielectric	4.3	177.8								
10		Plane	VSS	Conductive			33							
		Core		Dielectric	4.3	152.4								
11		Signal	Inner 11	Conductive			33	304.8	101.6	0.3	50.26	93.74	14.24	
		Prepreg		Dielectric	4.3	76.2								
12		Signal	Inner 12	Conductive			33	304.8	101.6	0.3	50.26	93.74	14.24	
		Core		Dielectric	4.3	152.4								
13		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
14		Signal	Bottom	Conductive			38	203.2	101.6	0.33	53.65	99.68		
		Soldermask		Dielectric	3.3	12.7								

"Prepared for mVia use"

A sixteen layer 1.6mm based on only 3 cores. This build is adapted for 5 microvias stacked or staggered. (1-2 / 2-3 / 3-4 / 4-5 / 5-6) and indentical (16----11)

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16 layer 1.6mm foil build, microvia via

UNITS: um — ICD STACKUP PLANNER FX – www.icd.com.au — 5/6/2014 — Total Board Thickness: 1562.8 um

Differential Pairs > New Pair

Layer No	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	12.7								
1	200 100 100 100 100 100	Signal	Top	Conductive			40	152.4	101.6	0.34	53.44	95.43		
		Prepreg		Dielectric	4.3	76.2								
2		Plane	GND	Conductive			33							
		Prepreg		Dielectric	4.3	127								
3		Signal	Inner 3	Conductive			33	203.2	101.6	0.3	42.58	81.75	51.03	
		Prepreg		Dielectric	4.3	76.2								
4		Signal	Inner 4	Conductive			33	203.2	101.6	0.3	31.95	62.43	51.03	
		Prepreg		Dielectric	4.3	76.2								
5		Plane	VDD	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
6		Signal	Inner 6	Conductive			15	254	101.6	0.17	40.85	80.54	57.49	
		Core		Dielectric	4.3	76.2								
7		Signal	Inner 7	Conductive			15	254	101.6	0.17	49.26	96.32	57.49	
		Prepreg		Dielectric	4.3	127								
8		Plane	VCC	Conductive			15							
		Core		Dielectric	4.3	101.6								
9		Plane	GND	Conductive			15							
		Prepreg		Dielectric	4.3	127								
10		Signal	Inner 10	Conductive			15	254	101.6	0.17	49.26	96.32	57.49	
		Core		Dielectric	4.3	76.2								
11		Signal	Inner 11	Conductive			15	254	101.6	0.17	40.85	80.54	57.49	
		Prepreg		Dielectric	4.3	76.2								
12		Plane	VSS	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
13		Signal	Inner 13	Conductive			33	203.2	101.6	0.3	30.81	60.69	45.33	
		Prepreg		Dielectric	4.3	76.2								
14		Signal	Inner 14	Conductive			33	203.2	101.6	0.3	30.81	60.69	45.33	
		Prepreg		Dielectric	4.3	76.2								
15		Plane	VCC	Conductive			33							
		Prepreg		Dielectric	4.3	76.2								
16		Signal	Bottom	Conductive			40	152.4	101.6	0.34	53.44	95.43		
		Soldermask		Dielectric	3.3	12.7								

Materials Comparation (Dk vs. F)

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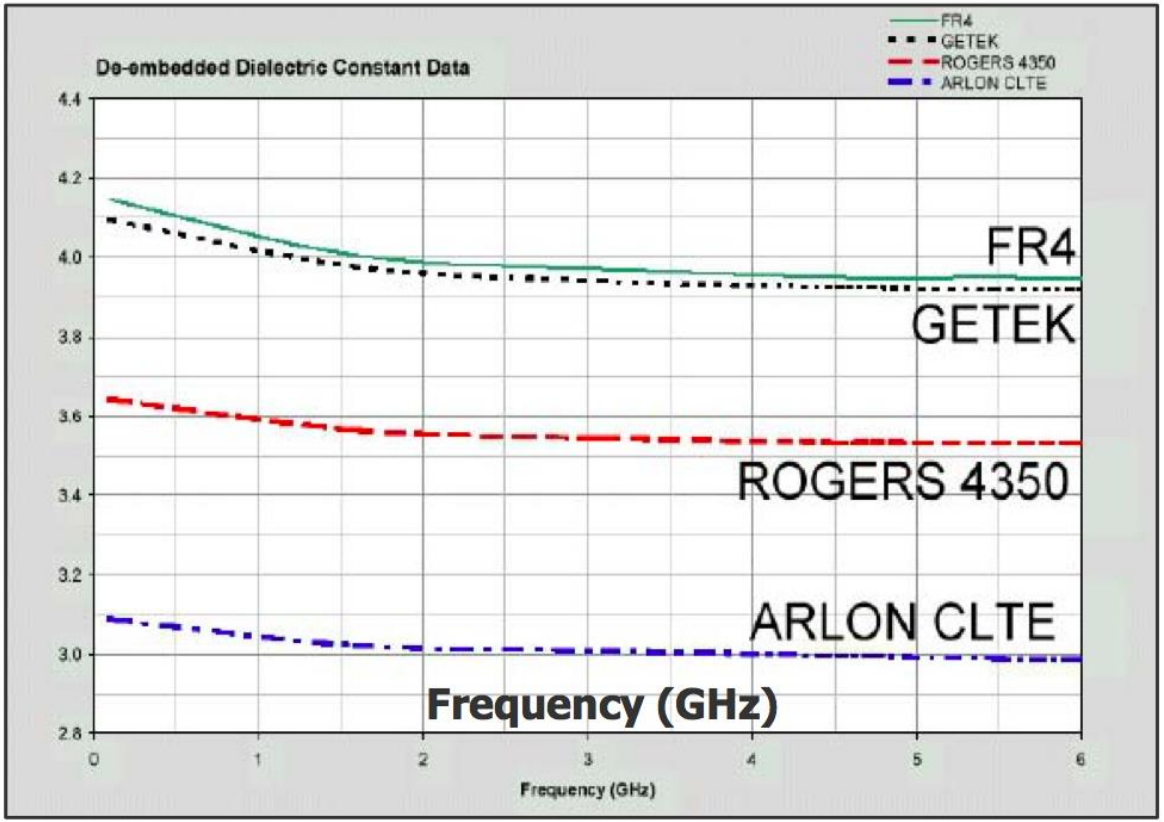

Morgan, Chad & Helster, Dave, "The Impact of PWB Construction on High-Speed Signals"DesignCon 99.

Dielec Constants vs. Frequency

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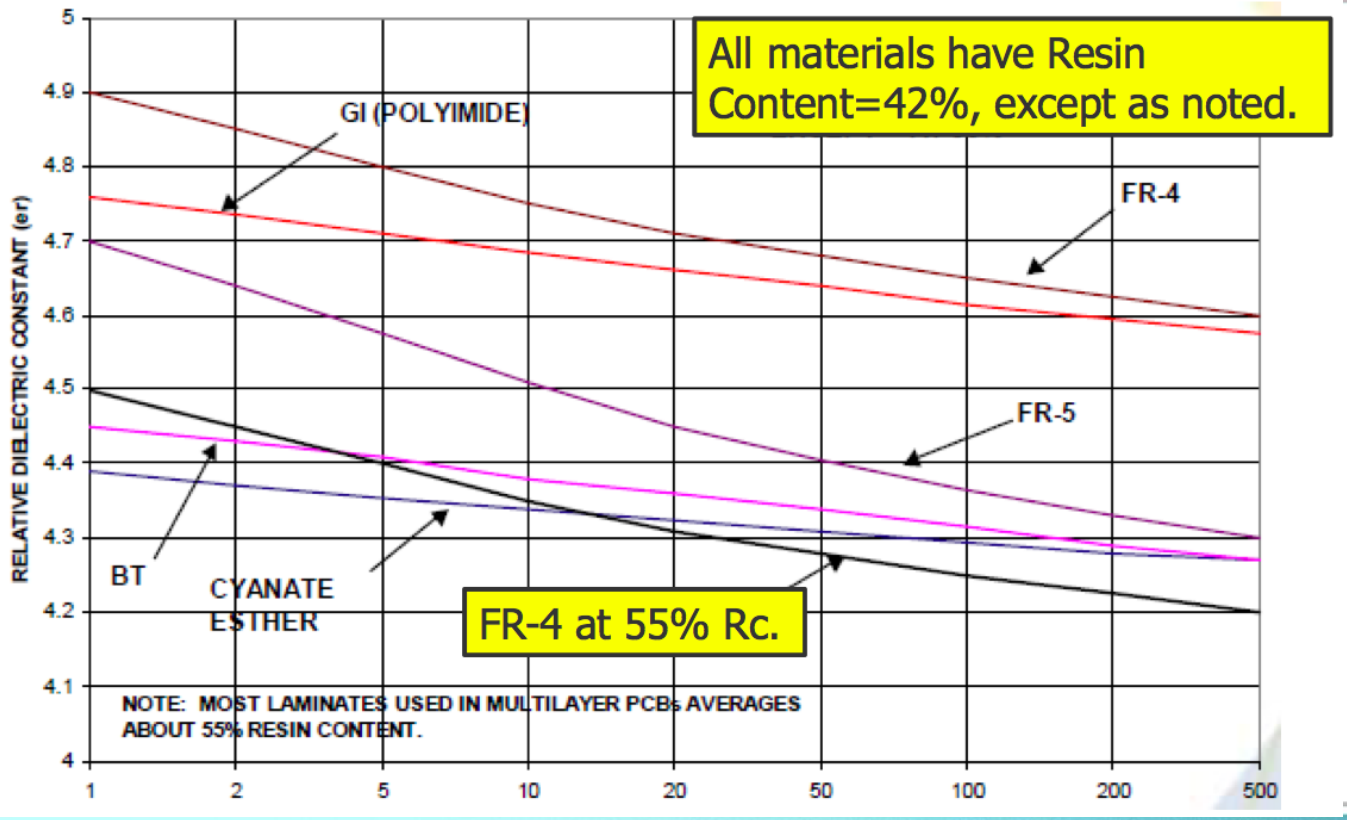

Copper Foil Types

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ED = Standard Shiny Copper, Copper Tooth
HTE = High Temp Elongation Shiny Copper, Copper Tooth
DSTF/RTF = Reverse Treat, Low Profile Copper Tooth
DT = Double Treat Copper, No Black Oxide Needed

- The RTF Copper Foils Offer Benefits To The Fabricator During Processing – More Defined Etched Line, Ability For Thinner Lines And Lower Copper Tooth Profile.

- **VLP/e-VLP/H-VLP** Foils Are Used For Better Impedance Control & Improved Signal Integrity

- 95+ % Of NA Is RTF Foil. Very Small Percentage = DT

- RTF Foil Use Increasing In Asia-Pacific Region

- Thicker Cores Still Use Some HTE Or ED Foil.

Copper Weights

18 micron = H oz
35 micron = 1 oz
70 micron = 2 oz

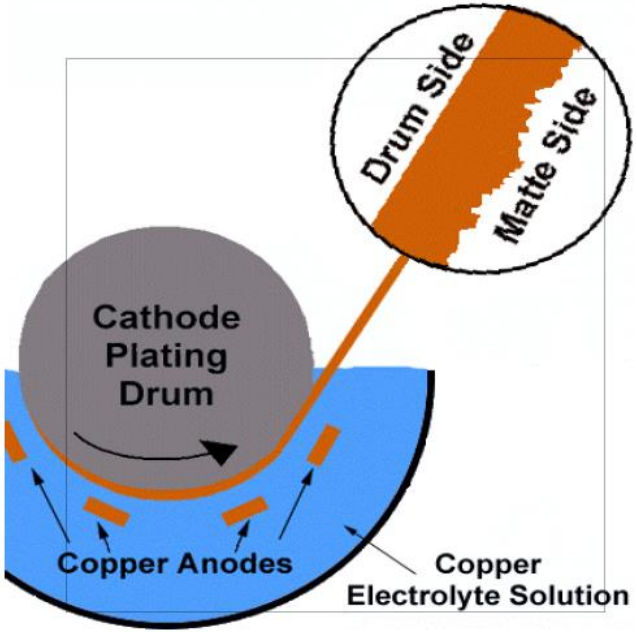
Heavier Copper Such As 3, 4 And 5 Oz Foil Used For Power Supply Designs Or Ground Planes In MLB Designs

5 and 6 oz Cu for Automotive 4 – L designs

12 oz Cu used for Automotive 2 – L designs

DSTF =
Drum Side Treat Foil

Copper Foil Manufacturing Process



Copper Roughness Specifications

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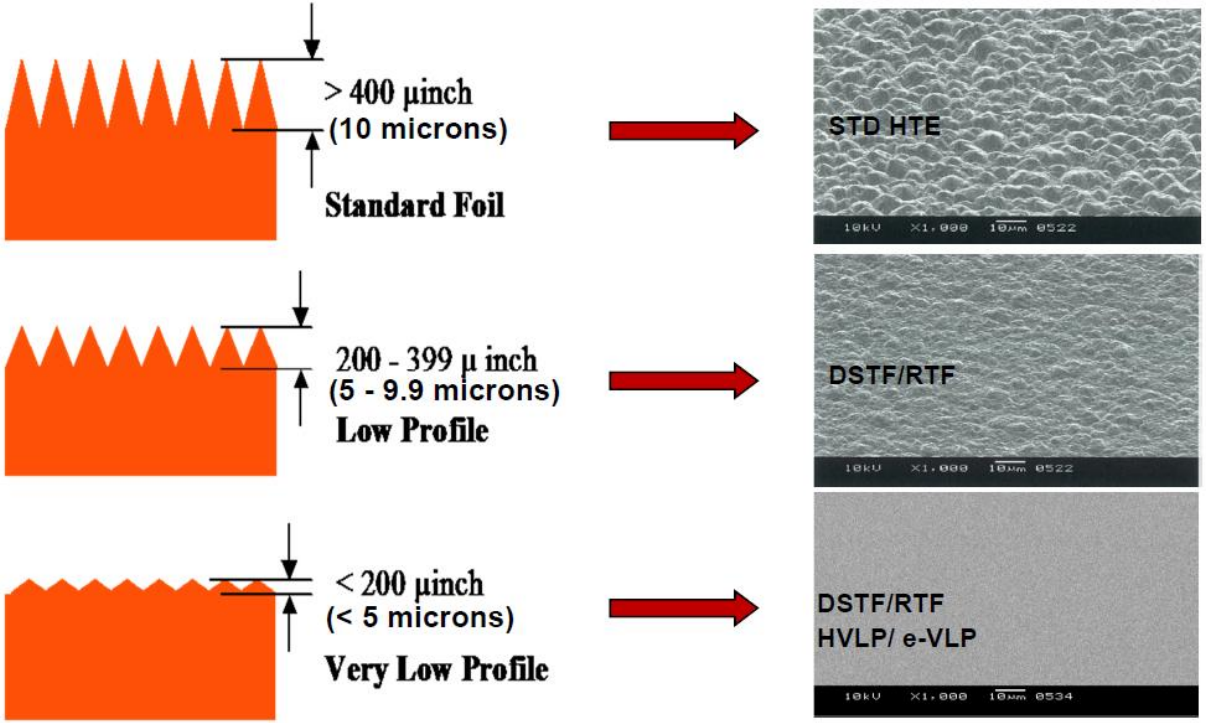

Materials

PCB Materials Properties

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Core Thickness	Standard Constructions	Resin Content	Dk 500 MHz	Dk 1 GHz	Dk 2.0 GHz	Dk 5.0 GHz	Dk 10.0 GHz	Df 500 MHz	Df 1 GHz	Df 2.0 GHz	Df 5.0 GHz	Df 10.0 GHz

- Core/Laminates and prepreg are known by:
  - — Manufacturer; e.g., Isola, Rogers, Nelco, etc.
  - — Thicknesses; e.g., 1.5 mils (Preg) vs. 60 mils (Core)
  - — Glass weave styles; e.g., coarse (7628) vs. fine (106)
  - — Resin systems; e.g., Epoxy, Polyimide, etc.
  - — Resin content (%); e.g., 32-69%
  - — Tg: Glass transition temperatures; e.g., 140 (Low Tg), 180 (Hi Tg), 280 C
  - — Dk: Dielectric Constant (Er, Relative Permittivity); 3.0-4.8
    - – A relative measure of a material's capacitance, or ability to store a charge, as compared to a vacuum (Er=1.0)
  - — Df: Dissipation Factor (AKA: Loss Tangent); 0.020-0.001
    - – A measure of the energy loss in a dielectric per unit length

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Materials

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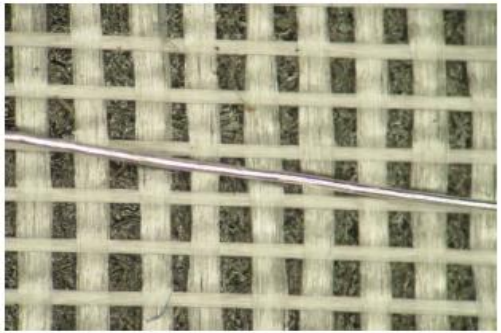
SOME REPRESENTATIVE GLASS STYLES



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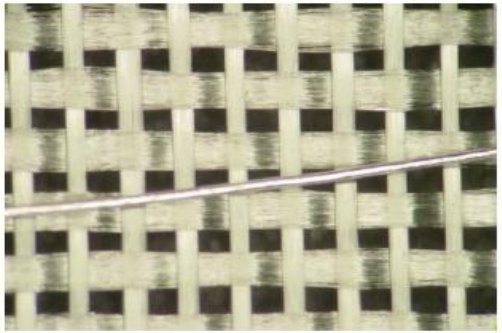
WIRE IS 3.5 MILS IN DIAMETER



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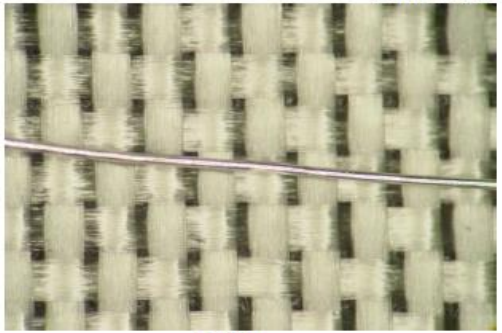

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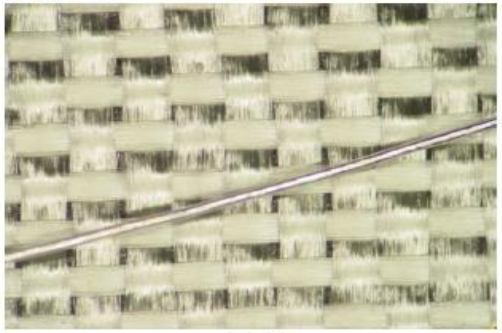

3313

Isola-group.com

Materials

IPC-4101D-WAM1

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Material Composition Keywords	All Appropriate Specification Sheets
BT / Epoxy / Woven Glass	/30, /135
Cyanate Ester / Woven Glass	/71
Cyanate Ester / Woven S-2 Glass	/70
Cyanate Ester / Woven Quartz	/61
Epoxy / Cyanate Ester / Woven Glass	/29, /72, /73
Epoxy / Non-Epoxy / Nonwoven Aramid	/58
Epoxy / Nonwoven Aramid	/55
Epoxy / Paper	/04
Epoxy / PPO / Woven Glass	/25, /103
Epoxy / Woven Aramid	/50
Epoxy / Woven Glass	/20, /21, /22, /23, /24, /26, /27, /97, /98, /99, /101, /121, /122, /124, /125, /126, /127, /128, /129, /130, /131
Epoxy / Woven Glass / Nonwoven Glass	/12, /16, /35, /81
Epoxy / Woven Glass / Paper	/10, /15, /80
Phenolic / Paper	/00, /01, /02, /03, /05
Polyester / Glass	/13
Polyester / Woven Glass / Nonwoven Glass	/11
Polyimide / Epoxy / Woven Glass	/42
Polyimide / Nonwoven Aramid	/53
Polyimide / Woven Glass	/40, /41, /43, /44
Polyimide / Woven Quartz	/60
PPE / Woven Glass	/90, /91, /96, /102

Materials

IPC-4101D-WAM1

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Description or Application Keywords	All Appropriate Specification Sheets
Additive / Semi-Additive	/80, /81
Composite	/10, /11, /12, /14, /15, /16, /35
Consumer Electronics	/00, /01, /02, /03, /04, /05, /10, /11, /12, /14, /15, /16, /80, /81
Crossplied Unidirectional	/27
Double-Sided	/12, /14, /16, /81
Heatsink Application	/31, /32, /33, /34, /35
Lead-Free FR-4	/99, /101, /121, /122, /124, /125, /126, /127, /128, /129, /130, /131
Lead-Free Non-FR-4	/16, /102, /103
Microvia	/53, /55, /58
Non-Reinforced Film	/31, /33, /34
Punchable	/00, /01, /02, /03, /04, /05, /10, /11, /12, /14, /15, /16, /80, /81
Single-Sided	/00, /01, /02, /03, /04, /05, /10, /11, /15, /80

Materials

IPC-4101D-WAM1

ELMATICA®

ANSI or Military Keywords	All Appropriate Specification Sheets
CEM-1	/10, /15, /80
CEM-3	/12, /14, /16, /35, /81
CRM-5	/11
FR-1	/02
FR-2	/03, /05
FR-3	/04
FR-4.0	/21, /24, /26, /27, /72, /73, /97, /98, /99, /101, /121, /124, /126, /129
FR-4.1	/122, /125, /127, /128, /130, /131
FR-5	/23
G-10	/20
G-11	/22
XPC	/00
XXXPC	/01
GFN	/21, /24, /97, /98
GFT	/26
GPY	/30, /40, /41, /42, /135

Materials

IPC-4101D-WAM1

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Material Property Keywords	All Appropriate Specification Sheets
CAF Resistance	/29, /30, /61, /70, /71, /72, /73, /102, /126, /129, /130, /131, /135
High Decomposition Temperature	/99, /124, /125, /126, /128, /129, /130, /131
High Reliability	/40, /41, /42, /43, /44
Hot Flex Strength	/22, /23
Low Dk / Df	/13, /25, /43, /44, /50, /53, /55, /58, /61, /70, /71, /72, /73, /90, /91, /96, /102, /103
Low Halogen Content	/05, /14, /15, /35, /44, /58, /96, /122, /125, /127, /128, /130, /131
Low X / Y CTE	/50, /53, /55, /58, /60, /61, /70
Low Z-axis CTE	/43, /44, /99, /101, /102, /121, /122, /124, /125, /126, /127, /128, /129, /130, /131
Non-Flame Retardant	/20, /22
Thermally Conductive	/31, /32, /33, /34, /35

Advanced HDI PCBs

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microvia holes , stacked and staggered , buried vias and buried holes

HDI Advantages

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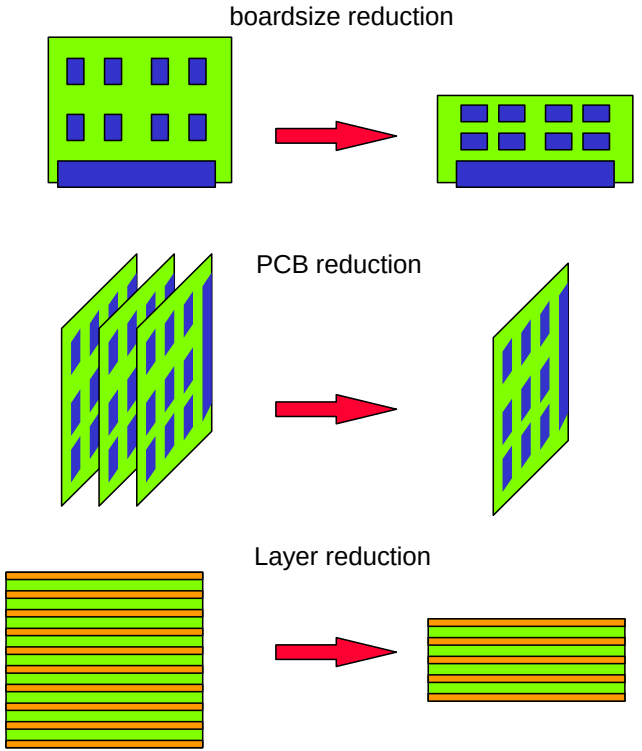
Although PCB price will increase by adding Microvias,
the total system costs can be reduced.



HDI Advantages

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- **Increasing Fan-out**
  - No lost routing space on innerlayers.
  - More routing space between pads.
- **Less risk during soldering process on;**
  - solder-bridge
  - solder paste flow away through via holes.
- **Advanced electrical properties**
  - Shortest possible connection
- **Advanced electrical properties**
  - Thermal Microvias

HDI Advantages

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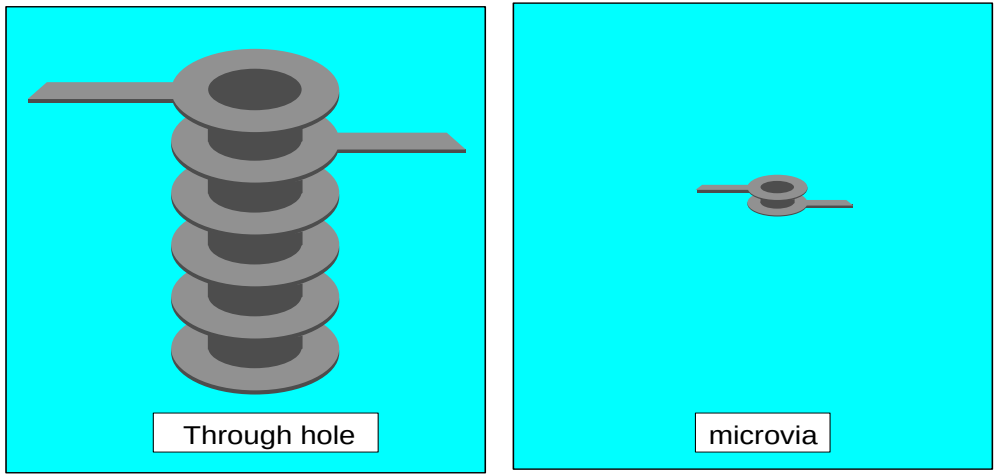
High Density Interconnect



High Inductance

Lower Inductance

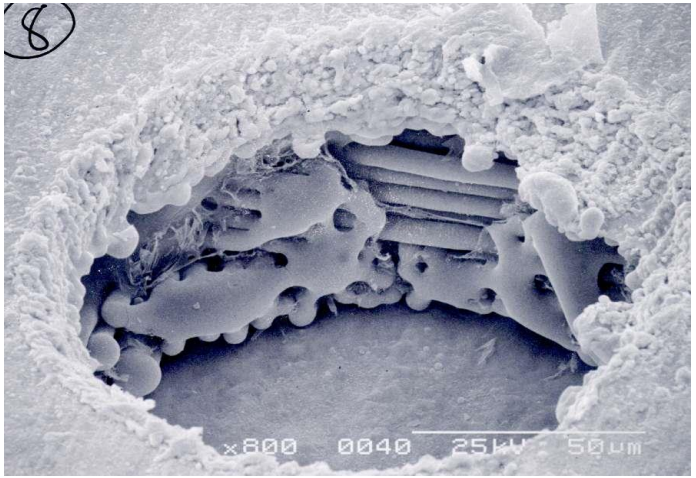
HDI Advantages

ELMATICA®

High Density Interconnect

Dual head Laser

- UV – copper ablating laser
- CO_2 – Dielectric ablating laser



Microvia under 800x magnification

HDI Advantages

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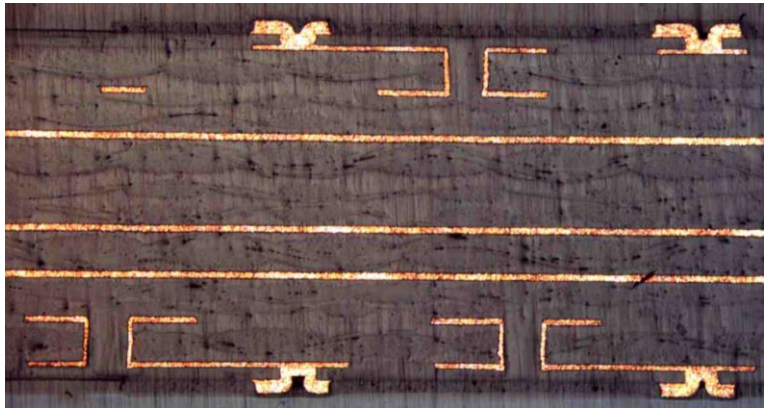
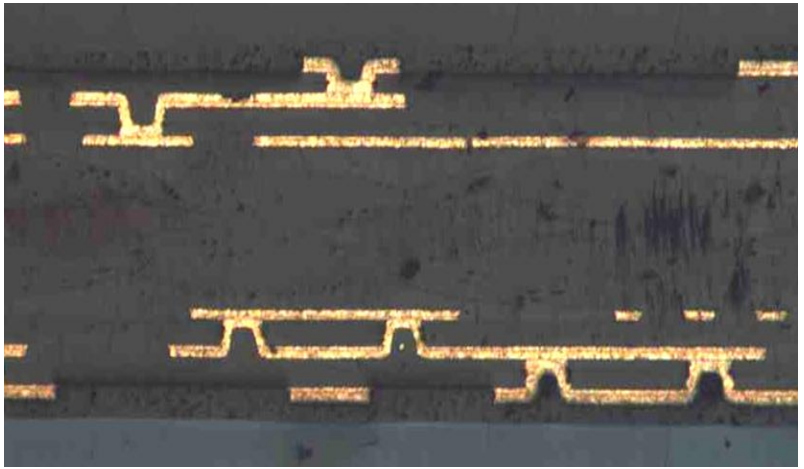
HDI Microsection



Lay up structure: 1+1+0+1+1



Lay up structure: 2+4+2

HDI Advantages

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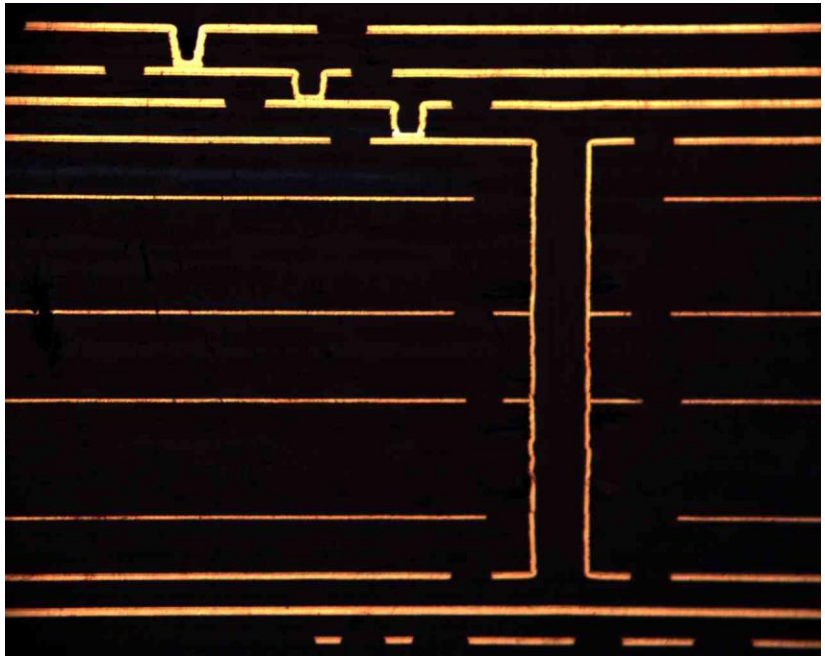
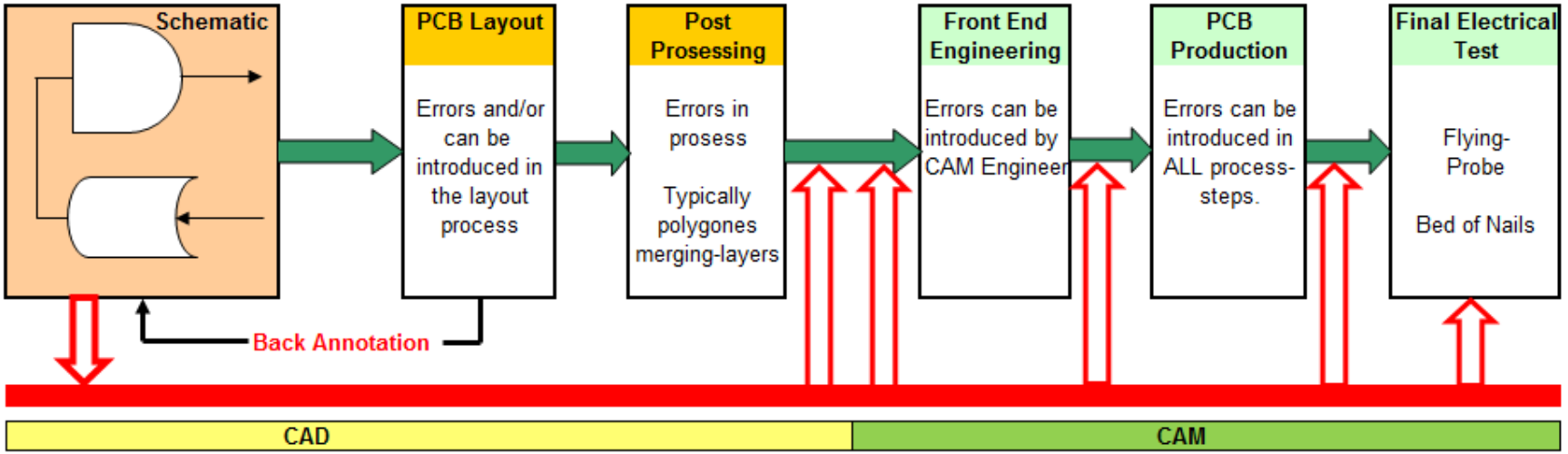
HDI Microsection
of a
12 layer PCB



Lay up structure: 3 + 6 + 3

IMPORTANS of NETLIST



Net list format: IPC D-356B

HDI Advantages

What to do when you need a stack up with impedance requirements:

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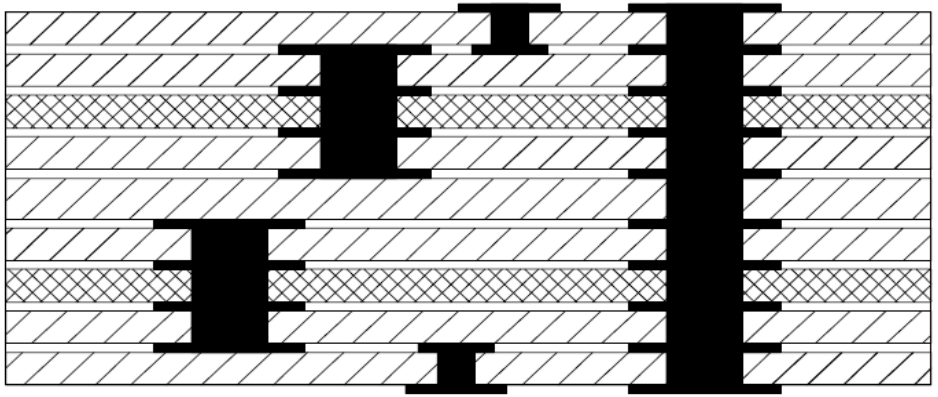
USAGE	
Components, signals	L1
Signals	L2
GND plane	L3
Signals	L4
GND plane	L5
PWR plane	L6
Signals	L7
GND plane	L8
Signals	L9
Components, signals	L10



Additional information:

- Final PCB thickness 1.6mm
- Single ended 50 ohms,
- 100 ohms differential,
- Prefered min track width is 0.127mm.

PCB Size: 110 x 70mm
Routed on Layer 1, 2, 4, 7, 9 & 10
Routed on layer 4 and 7.

HDI Advantages

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Changes in physical parameters will affect impedance as follows:

As Physical Values Change	Impedance Will Move
Dielectric Constant (DK) ↓	↑
Dielectric Thickness (h) ↑	↑
Line Width (w) ↓	↑
Line Thickness (t) ↓	↑

HDI Advantages **Effect of variables on impedance value.**

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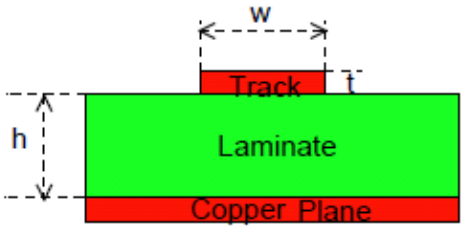
We can take a simple strip-line configuration, vary one element at a time, and calculate the resulting value.



$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4h}{0.67\pi(0.8w+t)}\right]$$

Er	w	h	t	Zo	Δ	
4.7	0.15 mm	0.5 mm	0.035 mm	50.18 Ω		
4.5				51.29 Ω	+ 1.10	±
4.9				49.15 Ω	- 1.03	2.1%
± 4.3%	0.175mm			46.82 Ω	- 3.36	±
	0.125mm			54.01 Ω	+ 3.82	7.2%
	± 16.7%	0.55mm		52.82 Ω	+ 2.64	±
		0.45mm		47.27 Ω	- 2.92	5.5%
		± 5.0%	0.025mm	52.03 Ω	+ 1.85	±
			0.045mm	48.45 Ω	- 1.73	3.6%
			± 28.6%			

HDI Advantages

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What to do when you need a stack up with impedance requirements: (Cont'd)

Feed back from manufacturer should be:

- Complete stack up, BOM.
- Track width to use on the impedance traces
- Space to use between the impedance traces
- Calculation result

Make your critical tracks visible and easy to find

- Use a dedicated D-Code for theese traces

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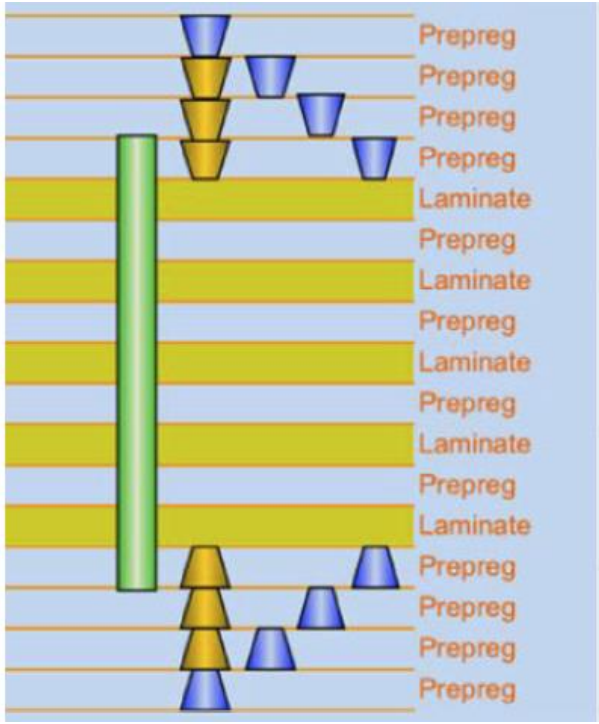
WUS - TW

HDI PCB Design Guide

2015 Q2

- HDI PCB Structure
- HDI PCB Design Guide
- PCB Design Suggestion
- Design for Manufacture



- +1 Stackup
- +2 Stackup
- +3 Stackup
- +4 Stackup
- Anylayer Stackup

HDI PCB Structure -1

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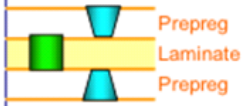
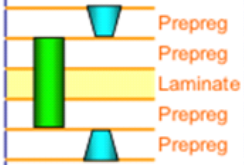
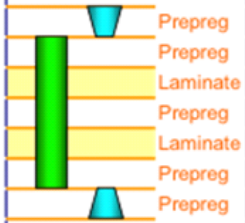
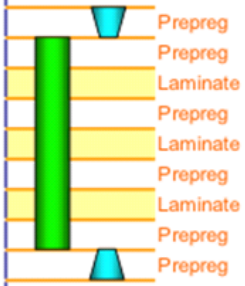
+1 Stackup

	1+2+1 HDI FCV	1+4+1 HDI FCV	1+6+1 HDI FCV	1+8+1 HDI FCV
				
Lamination	1	2	2	2
Pattern Etching	2	3	4	5
Plating	2	2	2	2
CFM / Laser drill	1	1	1	1
Mechanical drill	1	1	1	1
Buried via filling	1 (optional)	1 (optional)	1 (optional)	1

* PTH for tooling hole only, not recommend for inter-connect via.

HDI PCB Structure -2

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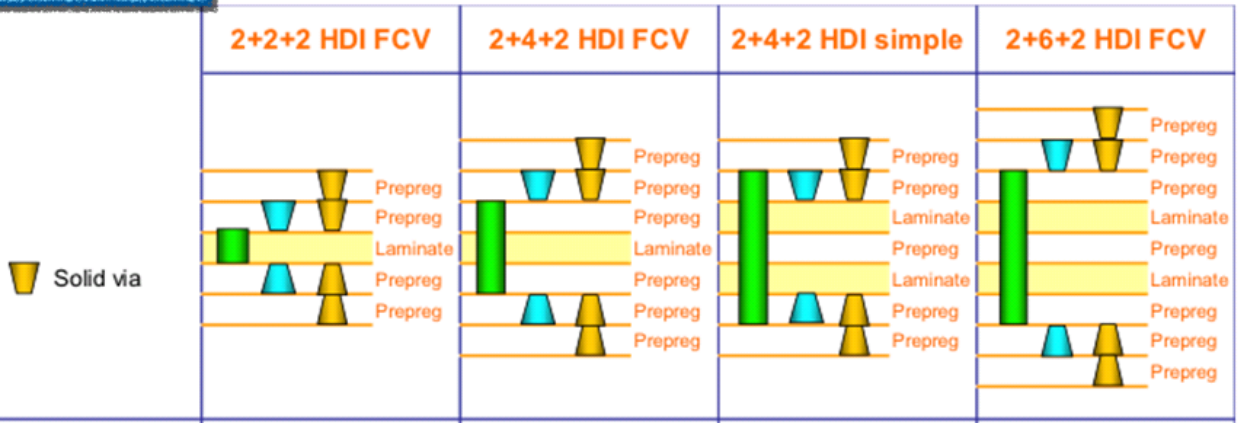
+2 Stackup

☑Main Stream



	2+2+2 HDI FCV	2+4+2 HDI FCV	2+4+2 HDI simple	2+6+2 HDI FCV
Lamination	2	3	2	3
Pattern Etching	3	4	4	5
Plating	3 (Solid via optional)	3 (Solid via optional)	2 (Solid via optional)	3 (Solid via optional)
CFM / Laser drill	2	2	2	2
Mechanical drill	1	1	1	1
Buried via filling	1 (optional)	1 (optional)	1	1

* PTH for tooling hole only, not recommend for inter-connect via.

HDI PCB Structure -3

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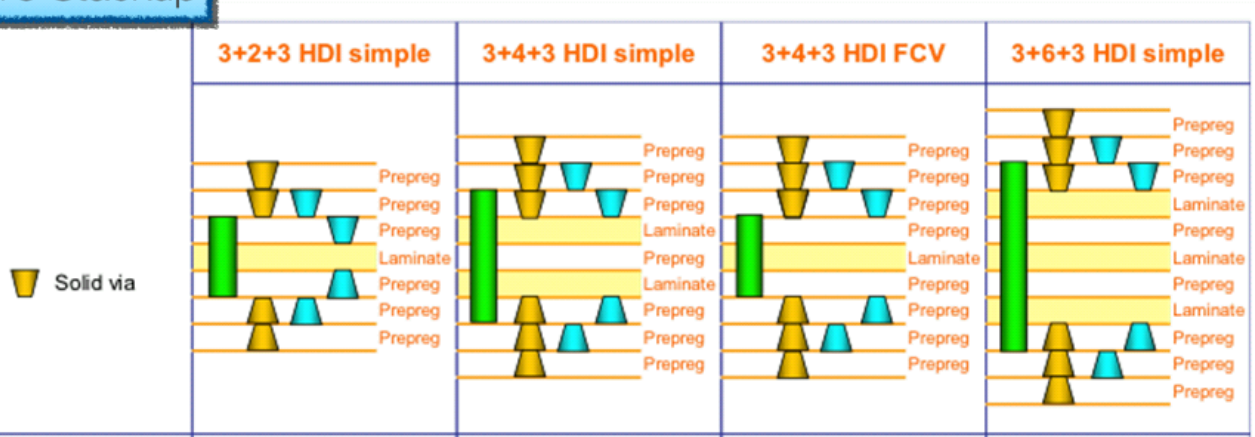
+3 Stackup

☑Main Stream



	3+2+3 HDI simple	3+4+3 HDI simple	3+4+3 HDI FCV	3+6+3 HDI simple
Lamination	3	3	4	3
Pattern Etching	4	5	5	6
Plating	3 (Solid via optional)	3 (Solid via optional)	4 (Solid via optional)	3 (Solid via optional)
CFM / Laser drill	3	3	3	3
Mechanical drill	1	1	1	1
Buried via filling	1 (optional)	1	1 (optional)	1

* PTH for tooling hole only, not recommend for inter-connect via.

HDI PCB Structure -4

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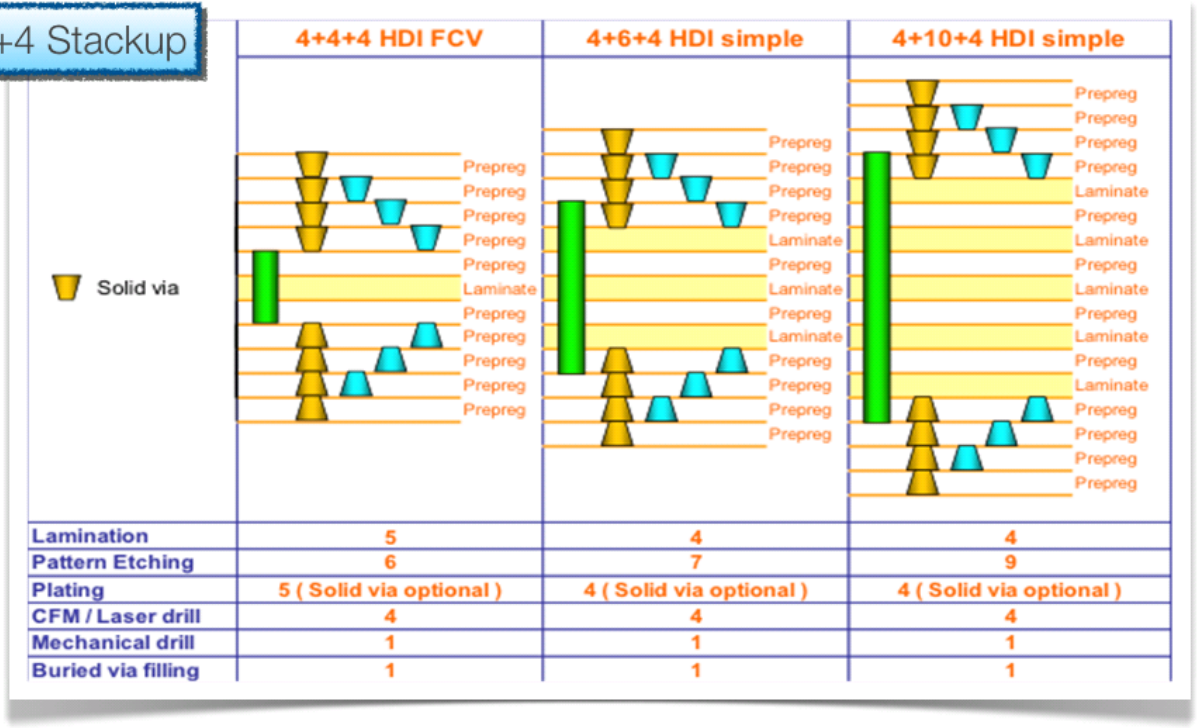
+4 Stackup



	4+4+4 HDI FCV	4+6+4 HDI simple	4+10+4 HDI simple
Lamination	5	4	4
Pattern Etching	6	7	9
Plating	5 (Solid via optional)	4 (Solid via optional)	4 (Solid via optional)
CFM / Laser drill	4	4	4
Mechanical drill	1	1	1
Buried via filling	1	1	1

* PTH for tooling hole only, not recommend for inter-connect via.

HDI PCB Structure -5

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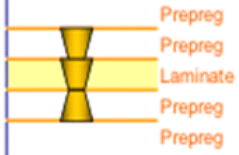
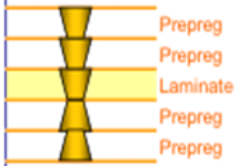
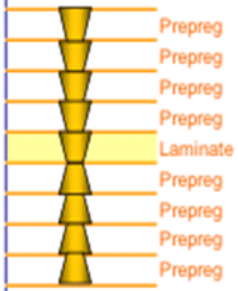
Anylayer Stackup	4L Anylayer	6L Anylayer	8L Anylayer	10L Anylayer
Solid via				
Lamination	1	2	3	4
Pattern Etching	2	3	4	5
Plating	2	3	4	5
CFM / Laser drill	2	3	4	5
Mechanical drill	0	0	0	0
Buried via filling	NA	NA	NA	NA
Board thickness	0.35~0.4mm	0.5~0.6mm	0.65~0.8mm	0.8~1.0mm

* PTH for tooling hole only, not recommend for inter-connect via.

HDI PCB Design Guide

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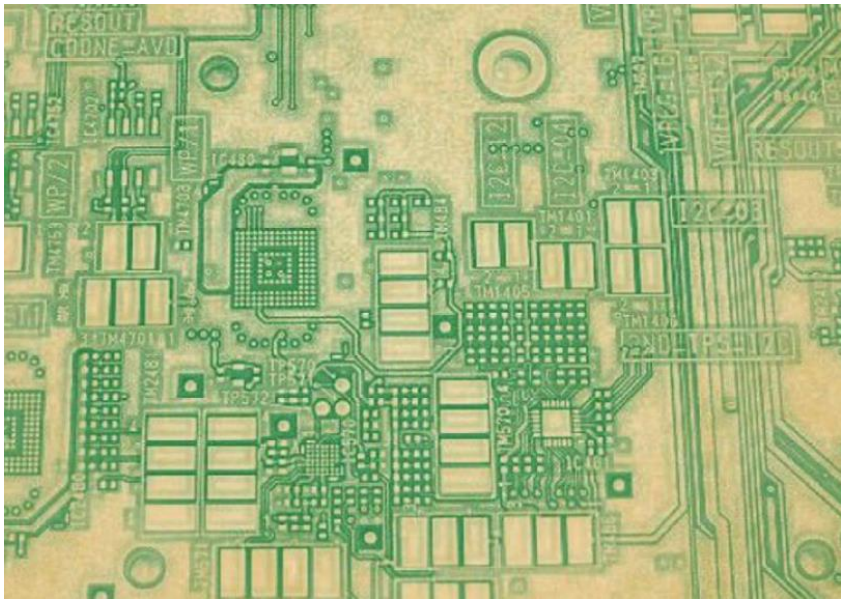

HDI PCB Design Guide -1

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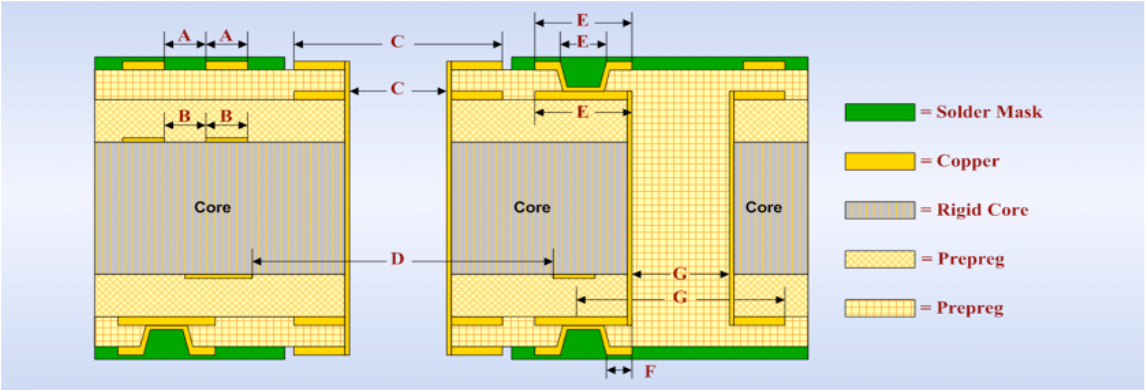

Unit: um

Sy.	Feature	Standard	Advanced
A	Min. LW/LS on plated layer	75/75	*50/50
B	Min. LW/LS - Cu foil (0.5 oz)	75/75	50/50
C	Min hole / land - PTH	250/500	200/400
C1	Max. aspect ratio for PTH	6	8
C2	Max. aspect ratio for PTH - Solid via	4	7
C3	POFV hole size (single hole size)	250~600	200~800

Sy.	Feature	Standard	Advanced
C4	Max. aspect ratio for POFV	5	7
D	Plane clearance on inner layer	FHS+500	FHS+400
E	Min. laser via/pad (capture/target)	125/300	100/225
E1	Max. aspect ratio for HDI layers	0.6	0.8
E2	Max. HDI dielectric thickness	70	80
F	Min. u via edge to buried via edge	150	125

* To support LW/LS 50/50 um, the surface copper thickness must be under 30 um (include copper plated).

HDI PCB Design Guide -2

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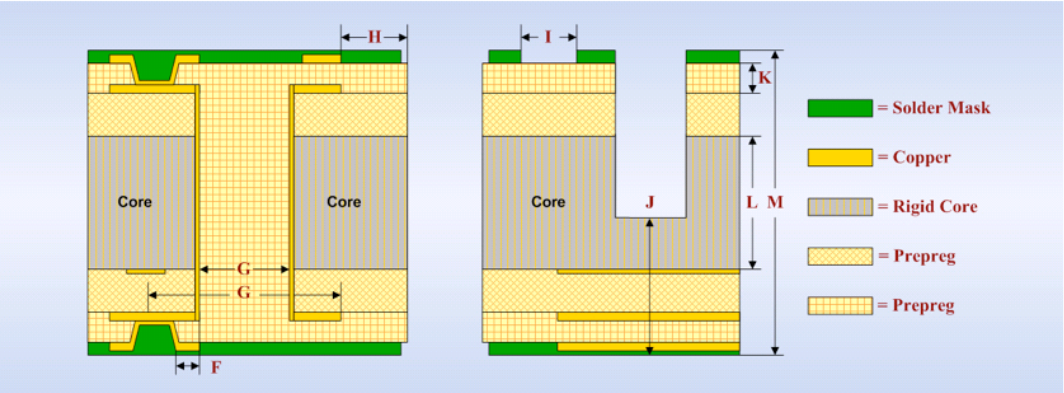

Unit: um

Sy.	Feature	Standard	Advanced
G	Min. hole/land - buried via	200/400	**150/350
H	Min. conductor to unplated hole	250	200
I	Min. soldermask opening size	200	150
J	Control Depth Rout tolerance	+/- 50	+/- 25
K	Max. HDI dielectric thickness	70	80
L	Min. core thickness - non-plated	75	50

Sy.	Feature	Standard	Advanced
L1	Min. core thickness - plated	75	65
M	Max. board thickness (mm)	2	2.4
M1	Min. board thickness (mm) - 1+2+1	0.4	0.35
-	SM registration	38	30
-	Max. layer count	14L	22L
-	Rout / V_cut outline tolerance	125	100

** The 150 um mechanical drill just can be applied to the limited thickness which is not more than 750 um.

Mechanical Tolerance Capability

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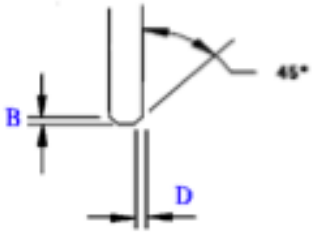
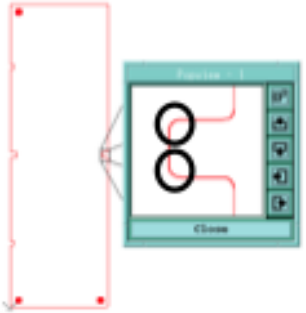
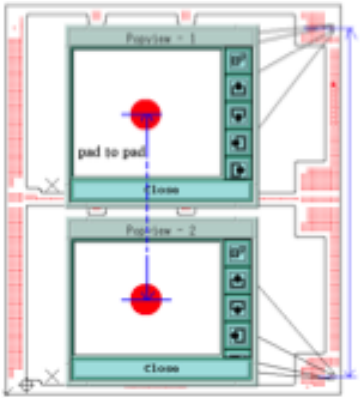




inside corner



	Process	Standard	Premium
	Routing		
1	Slot width of outline	2.0mm	0.8mm
2	Tolerance of outline	+/- 0.125mm	+/- 0.1mm
3	Min. inside corner	R0.6mm	R0.4mm
	V-cut		
4	Tolerance of position	+/- 0.125mm	+/- 0.1mm
5	Tolerance of residual thickness	+/- 0.125mm	+/- 0.1mm
	Bevel for Gold finger		
6	Board thickness	0.6~2.4mm	
7	Bevel angle	20 / 30 / 45 degrees	
8	Tolerance of dimension B and D	+/- 0.125mm	+/- 0.1mm
	Drilling		
9	Drill bit	0.2~6.35 mm	0.15 mm min.
10	Drill bit (for oval hole)	0.4~1.55mm	
11	Preciseness of hole location	+/- 0.075mm	
12	Tolerance of PTH diameter	+/- 0.075mm	+/- 0.05mm
13	Tolerance of NPTH diameter	+/- 0.05mm	+0.05 /-0.025mil
14	Hole to hole	+/- 0.075mm	
	Etching		
15	Pad to pad	+/- 0.075mm	+/- 0.06mm

RoHS Compliant Surface Finish

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Available Finish	Thickness	Chemical Supplier
OSP (Entek)	0.3 ~ 0.5 um	Enthone CU106AX
HT OSP	0.2 ~ 0.35 um	Shikoku - F2LX
HASL (Lead Free)	1 ~ 38 um	-
Immersion Tin	0.8 ~ 1.2 um	ATOtech
Immersion Ag	0.1 ~ 0.5 um	MacDermid
Electroless Ni/Au (ENIG)	Au: 0.05 um Ni: 3 ~ 6 um	DOW / ATOtech
Electroless Ni/Au + OSP	Au:0.05um / Ni:3~6um HT OSP: 0.2~0.35 um	-
Electroless Ni/Au + Au finger	Au:0.05um / Ni:3~6um Au finger: 0.25 ~ 1.25 um	Gold finger - GMF
OSP + Au finger	HT OSP: 0.2~0.35 um Au finger: 0.25 ~ 1.25 um	-
Immersion Ag + Au finger	Immersion Ag: 0.1~0.5um Au finger: 0.25 ~ 1.25 um	-
Electroless Bondable Au	0.2 ~ 0.8 um	Okuno / JX
ENEPIG	Pd:0.1um / Ni:3~8um Au : 0.1 um	UYEMURA

PCB Design Suggestion

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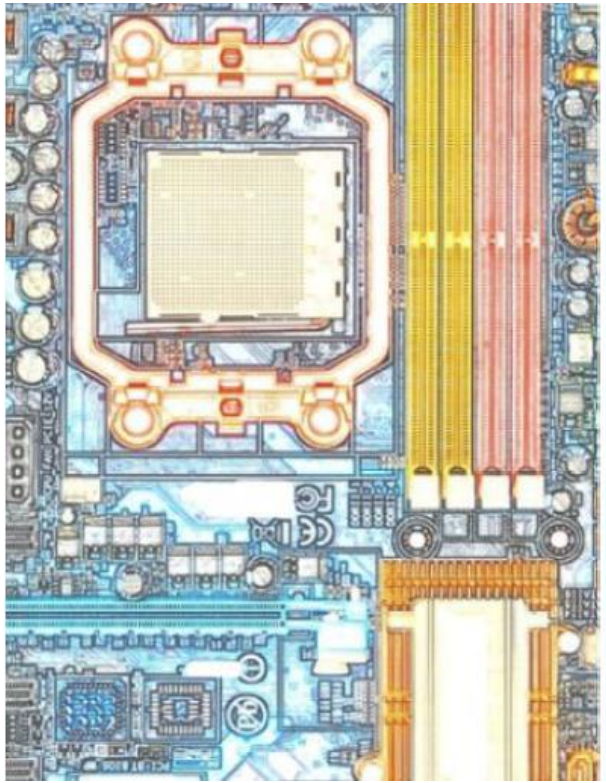

- P0.5mm BGA design
- P0.4mm BGA design
- P0.35mm BGA design
- LD and buried via design
- LD Solid via design
- Non-PTH design
- Cu and SM defined PAD
- 01005 design

PCB Design Suggestion

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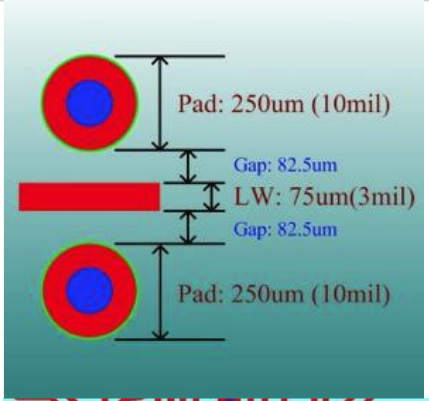
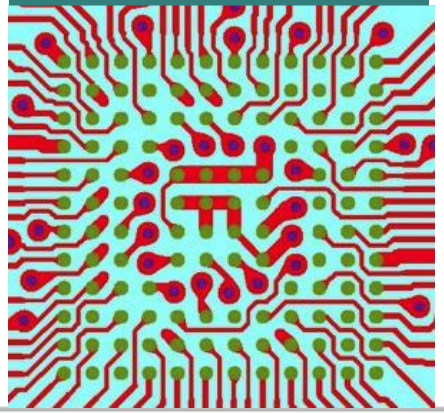
Trace goes through pads of P0.5mm BGA

- ☑ Cu Pad = 0.25 mm
- ☑ Trace width = 0.075 mm
- ☑ uVia dimeter= 0.1 mm
- ☑ Keep single trace in the middle between two BGA pads.





PCB Design Suggestion

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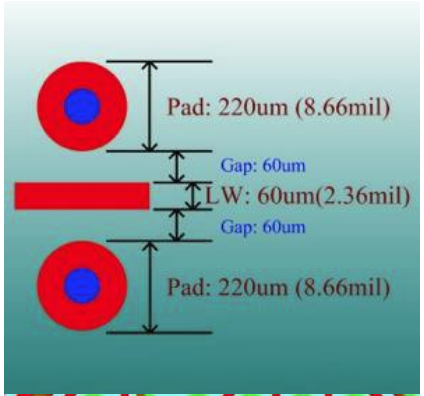
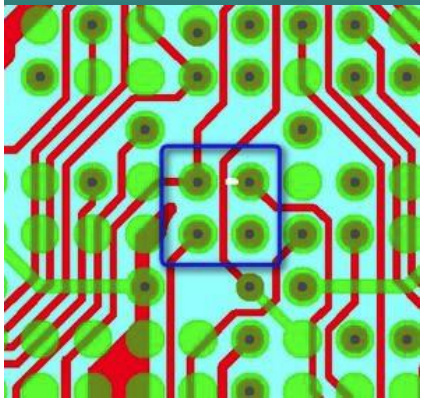
Inner layer trace goes through pads of P0.4mm BGA.

- Cu Pad = 0.22 mm
- Trace width = 0.06 mm
- uVia dimeter= 0.1 mm
- Keep single trace in the middle between two BGA pads.
- The Cu thickness must be less than 0.028 mm (1.1 mil).
- The cost of thinner trace is higher.

(This design just for inner layer)



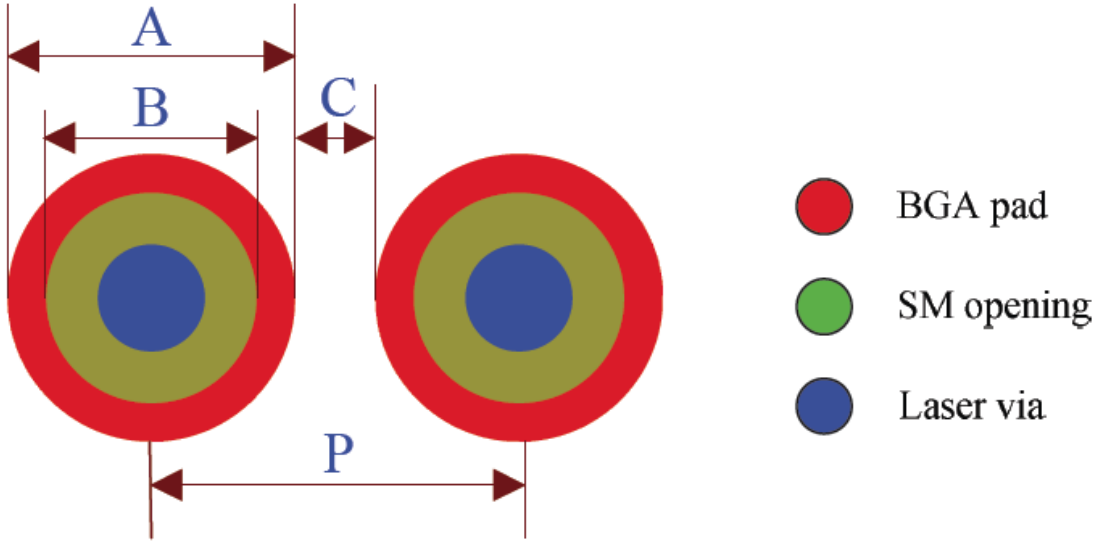


PCB Design Suggestion

ELMATICA®

0.35mm BGA pitch Layout suggestion.

- Pads are defined by Solder mask.
- uVias need Cu filled.



BGA pitch (P)	BGA pad (A)	SM opening (B)	Cu pad to pad (C)
0.35mm / 13.78mil	0.274mm / 10.78mil	0.2mm / 7.87mil	0.076mm / 3mil

PCB Design Suggestion

ELMATICA®

Design suggestion for staggered uVia & Buried via

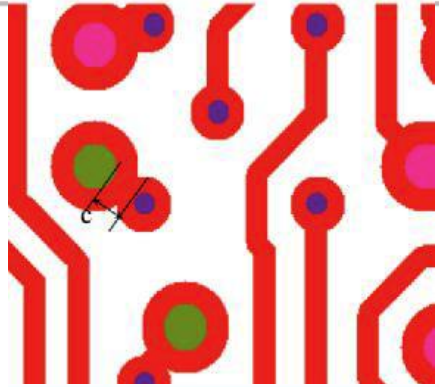
a. Buried via size : 0.2mm (0.15mm min.)

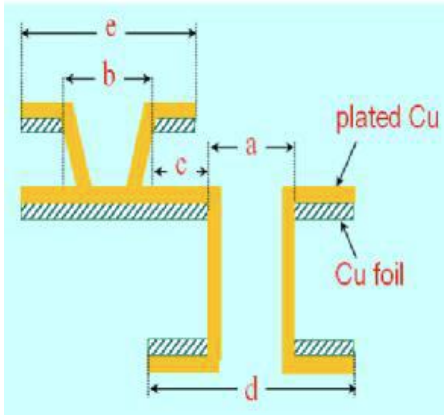
b. uVia size : 0.125mm (0.1mm min.)

c. Distance between buried via edge to uVia edge : **0.125mm min**.

d. Buried via pad size : 0.45mm (0.4mm min.)

e. uVia pad size : 0.3mm (0.25mm min.)





PCB Design Suggestion

ELMATICA®

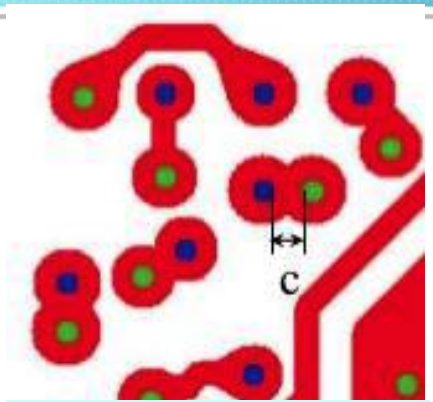
Design suggestion for staggered uVia & Buried via

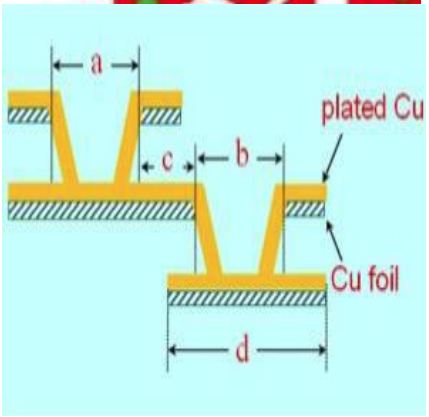
a. Top layer uVia size : 0.125mm (0.1mm min.)

b. BTM layer uVia size : 0.125mm (0.1mm min.)

c. Distance between uVia edge to uVia edge : **0.1mm min**.

d. uVia pad size : 0.3mm (0.25mm min.)





PCB Design Suggestion

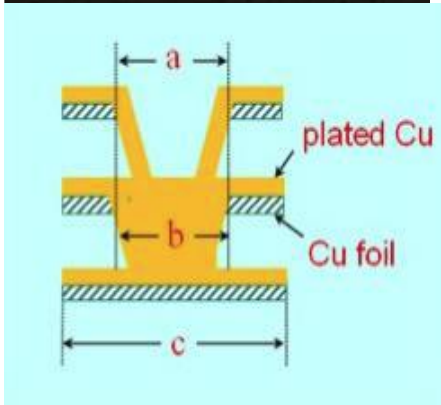
ELMATICA®

Design suggestion for stacked uVias

a. Top layer uVia size : 0.125mm (0.1mm min.)

b. BTM layer uVia size : 0.125mm (0.1mm min.)

c. uVia pad size : 0.3mm (0.25mm min.)

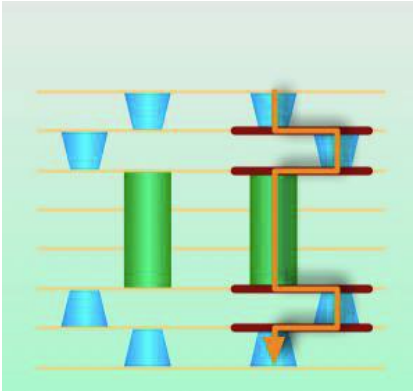


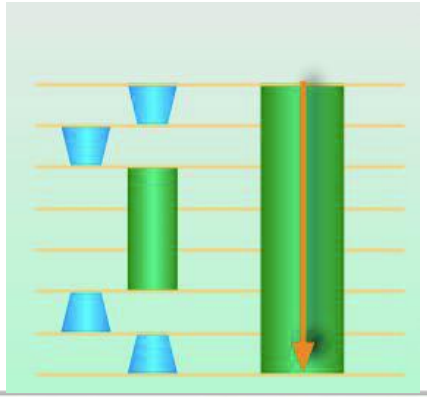
PCB Design Suggestion

ELMATICA®

Advantage of Non-PTH design.

- More space for layout usage on outer layer due to small pad size of uVia.
- Shorten processes, reduce lead time.
- Better surface Cu thickness control and more compliant with solid via requirement on outer layer.
- The PTH points to the interconnection via which is less than 20 mil.



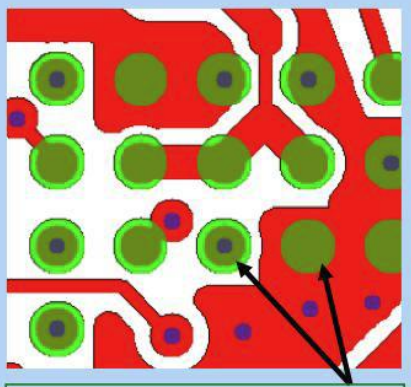


PCB Design Suggestion

ELMATICA®

Design Suggestion for BGA Layout

- ☑ Don’t mix the Metal defined and SM defined on the same BGA area. This would cause different pad size and may have an impact when assembly. Or shrink the SM open for ground ball pad to keep the same solder area.
- ☑ Put the microvia on the center of the BGA pad (metal defined pad).



Different area for Copper defined and SM defined pad

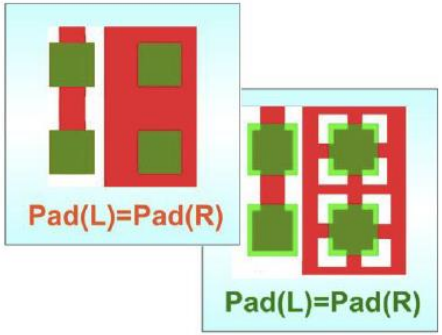
Red: pattern
Green: SM opening
Blue: micro via

PCB Design Suggestion

ELMATICA®

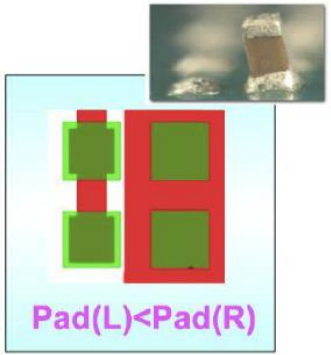
Design Suggestion for fine Chip layout

Do



- The SMD PAD with the same define (both pads with solder mask define or copper define).

Don't

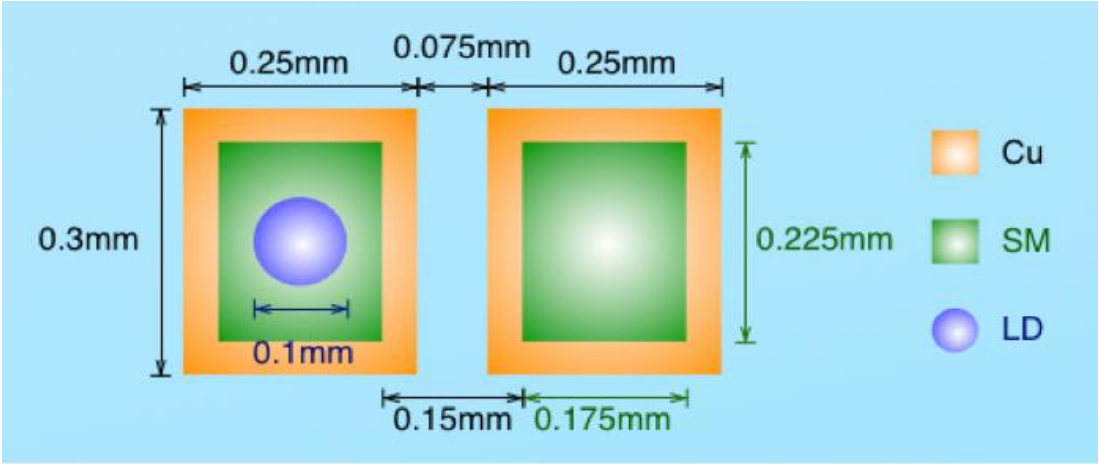


- The SMD PAD with different define (left pad with copper define, right pad with solder mask define).

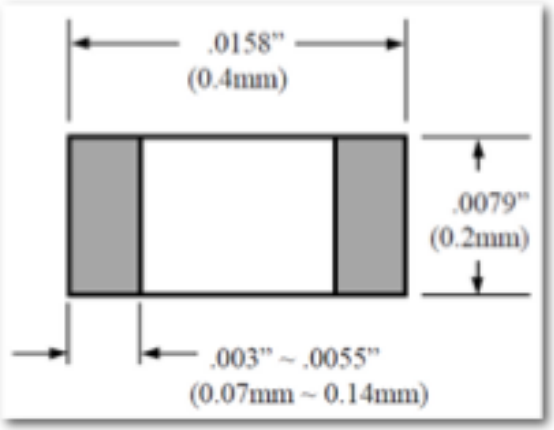
PCB Design Suggestion

ELMATICA®

01005 layout suggestion (with SM dam)



- Pads are defined by Solder mask.
- uVias need Cu filled.
- The surface copper thickness must be under 0.036mm.



Design for Manufacture

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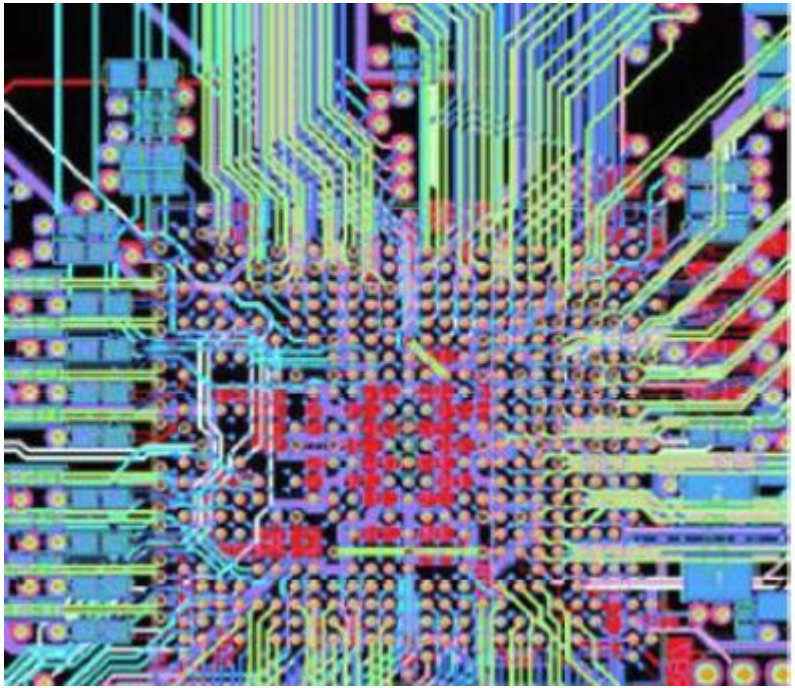


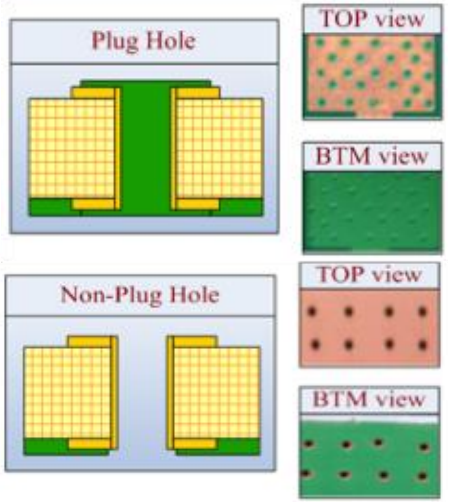
- Plug through Via
- Oval hole
- Legend

Design for Manufacture

ELMATICA®

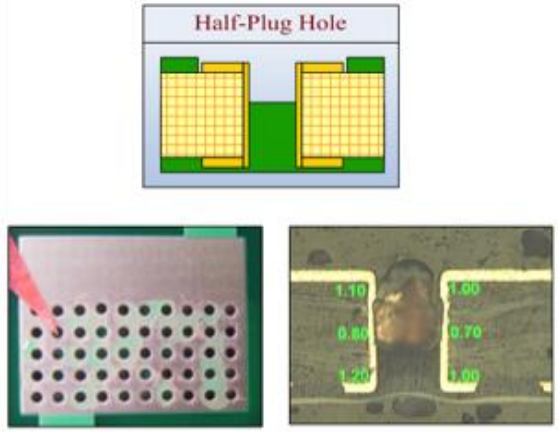
DFM => Plug Through Via

Do



- Exposed or Covered with SM on both sides
- Ensure the via quality

Don't



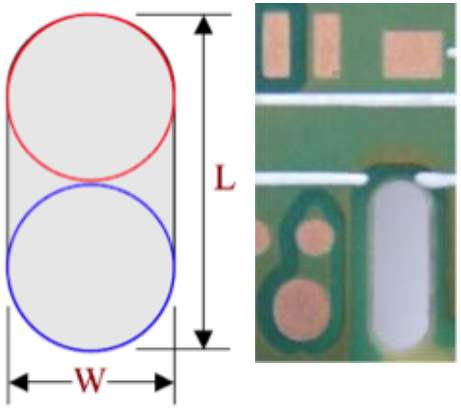
- Covered with S/M only on one side
- Potential risk of S/M residual and chemical corrosion.

Design for Manufacture

ELMATICA®

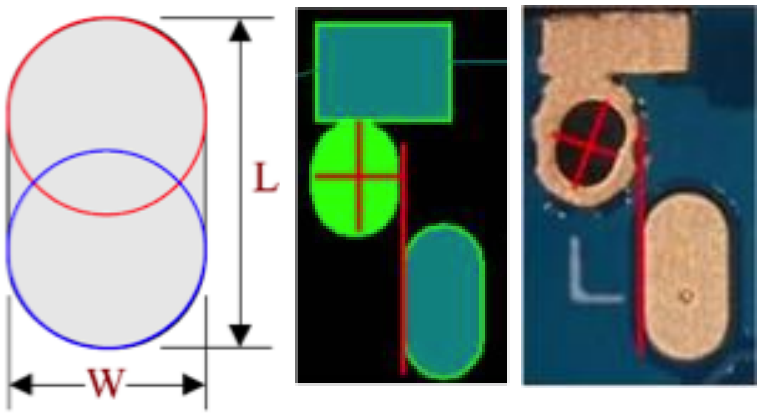
DFM => Oval hole

Do



- L >= W*2
- Ensure the oval hole shape quality

Don't



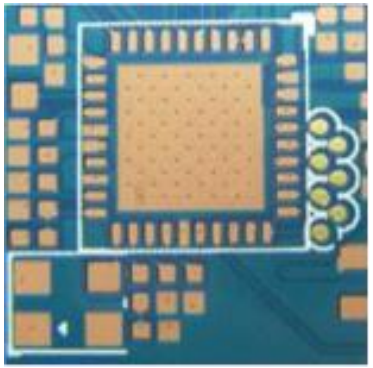
- L < W*2
- Potential risk of oblique oval hole

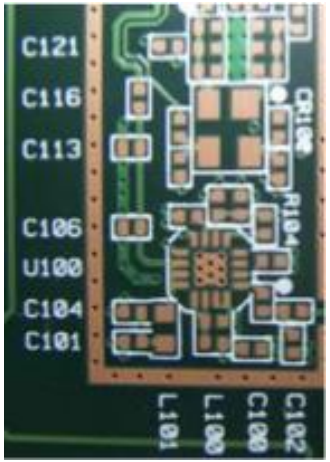
Design for Manufacture

ELMATICA®

DFM => Legend

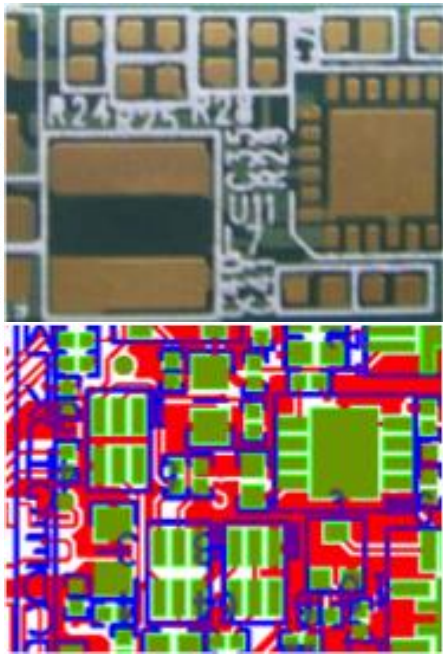
Do





- Height x Width 0.75x0.5mm min.
- Line width 0.115mm min.
- Distance between legend and copper exposed area 0.15mm min.

Don't



- Complex & unclear

the end

If you want to hear more of this, send me an email, and Elmatica will arrange somthing for you and your company

josse@elmatica.com