Product abstracts for Stockholm and Copenhagen, FPGAworld 2015

Title: Unlocking the full potential of 'in-lab' FPGA debug and verification.
Presenter: Frédéric Leens, CEO, Exostiv Labs
Abstract: Using actual FPGA board 'in the lab' for debug and verification is very common to explore debug cases requiring extended system service times and to overcome potential environment modeling issues. However, with the evolution of FPGA complexities, debugging 'in the lab' is sometimes disregarded - mainly because it does not offer sufficient visibility.
This session explores the trade-offs of using in-lab FPGA verification in conjunction with other techniques. It shows when using FPGA 'in the lab' is truly useful to reduce the overall debug and verification process and what has to be improved to do so.
Finally, it introduces EXOSTIV™, Exostiv Labs' flagship solution, that offers up to 200.000 times more visibility than standard embedded instrumentation during in-lab FPGA debug.

Title: **Optimizing HW/SW partition of a complex embedded system using C/C++**
Presenter: Olivier Tremois, EMEAI DSP Specialist FAE, Silica
Abstract: Xilinx® Zynq® All Programmable SoC brings ARM® SoCs and FPGAs together in a single die allowing ‘any-to-any’ connectivity and coprocessor acceleration for performance critical functions. The single-die integration allows efficient HW-SW partition and data com. However, designing an optimal system for such heterogeneous systems can be difficult and time-consuming. This talk introduces Xilinx SDSoC™ Development Environment which enables significant productivity improvements for emb SW product development on Xilinx Zynq systems using a C/C++ env

Title: **UVM Framework – an easy way to improve your verification job**
Presenter: Stefan Bauer (Mentor Graphics)
Abstract: Advanced verification methodologies like UVM (Universal Verification Methodology) enable higher level efficiency and re-usable structure. However many product teams do not take such productivity and quality benefits because they overestimate the ramp-up time required to introduce UVM. In order to increase the time-to-productivity Mentor Graphics created a framework. The so called UVM Framework provides a set of common UVM based testbench building blocks that are ready to use without the necessity of detailed UVM knowledge. In this session you will get a short overview of the UVM Framework followed by a live-demo.

Title: **Designing power for FPGAs**
Presenters: Thomas Ginell and Nicolai Mahncke - Field Application Engineer at Linear Technology
Abstract: Analysing the power requirements and planning the voltage rails to get an efficient and reliable solution is one of the key challenges in FPGA design. With this presentation, Linear Technology will show you how _LTpowerPlanner_ helps obtain, at the same time as it documents, the total solution without adding effort. Dynamic load response and output impedance is often the most important but also the most difficult behaviour to analyse; a guide to optimise it will be shown. By attending this seminar, you will learn how to find the best tools and documentation to help you design power for FPGAs.

Title: SmartFusion2 – Embedded system "Root-of-Trust" Secure Boot Demonstration
Presenters: Peter Trott, Field Application Engineer at Microsemi
Abstract: With the enhanced security that has been added to SmartFusion2, the family can not only be programmed in an “un-trusted” location but can also be used as a system root of trust device. Using secure cryptography techniques SmartFusion2 can be used to boot and validate code belonging to any processor within the system. If tampering is detected then action can be taken which far exceed any other security device that might be used within a system. This paper will show a possible implementation of secure boot and demonstrate the process on a hardware platform.

Title: Max10 - The next step in low cost FPGA integration
Presenters: Nikolay Rognlien, MDE Programmable Logic, Arrow Norway AS
Abstract: Learn about Altera’s offerings and how the unique Max10 device family may help provide higher Integration, increased Design Flexibility and lower system cost for your new designs.

Title: FPGA BASED CAN FD COMMUNICATION BRINGS CAN TO NEW LEVELS
Presenters: Ludvig Vidlid
Abstract: Since its birth some thirty years ago, the Controller Area Network (CAN) has become widely used especially, but not exclusively, in the automotive industry. Also since the birth of CAN, more and more controllers are connected to the bus, making its limited bandwidth a problem. In response to this CAN with Flexible Data-Rate (CAN FD) was first introduced a few years ago. We will discuss the enhancements made for CAN FD, the problems associated with it, and the motivation for implementing a CAN FD controller on an FPGA.