08:30	**FPGAworld 2015** **Registration; Stockholm, Sep 8th, Frösundaleden 2A, 169 70 Solna, SWEDEN.** **www.FPGAworld.com**		
Sponsors: 			
09:00	**Conference Opening** Thony Johansson, ÅF and Lennart Lindh, FPGAworld Room: Renen		
09:15 – 10:00	Keynote Speaker: **Ahmed Hemani**, Professor, KTH, Stockholm, Sweden **Next Generation Massively Parallel VLSI Architectures and Design Methods** Session Chair: Lennart Lindh, FPGAworld Room: Renen more information		
10:00	**Coffee Break & Exhibition, sponsor** EXOSTIV LABS		
10:30 - 12:30	Industrial&Student/Hackers Session Chair: **Roger Ericsson**, ÅF, Sweden Room: Renen Abstracts-A	Academic Program, B1-4 Session Chair: **Johnny Öberg**, KTH, Sweden Room: Räven Abstracts-B and Proceedings	Product Program Session Chair: **Ove Boström**, FPGAworld Room: Gasellen Abstracts-C
	A1: **Automotive ADAS feature saves lifes with flexible HW (FPGA etc.) – practical implementation reference** Tryggve Mathiesen, Qamcom R&T AB, Sweden A2: **High-speed FPGA-based stereovision system - a success story** Rafal Kapela, Ph.D.,Antmicro Ltd/Poznan University of Technology, Poland A3: **Real-time operating system, hardware or software?** André Norberg, AGSTU, Sweden, more information A4: **The critically missing VHDL testbench feature - Finally a structured approach** Espen Tallaksen, Bitvis, Norway more information	B1: **Analysis of FPGA-Based Reconfiguration Methods for Mobile and Embedded Applications** Darshika Gimhani Perera, University of Colorado, USA B2: **An EG-LDPC Based 2-Dimensional Error Correcting Code for Mitigating MBUs of SRAM Memories** Enver Cavus, Turkey B3: **High Level Synthesis Based Hardware Accelerator Design for Processing SQL Queries** Gorker Alp Malazgirt, Bogazici University, Turkey B4: **Comparison of Predictive-Corrective Video Coding Filters for Real-Time FPGA-based Lossless Compression in Multi-Camera Systems**	C1: **Unlocking the full potential of 'in-lab' FPGA debug and verification** Frédéric Leens, CEO, Exostiv Labs C2: **Designing power for FPGAs**, Thomas Ginell - Field Application Engineer at Linear Technology C3-4: **UVM Framework – an easy way to improve your verification job** Stefan Bauer (Mentor Graphics), InnoFour, (more information)

		Yimu Wang, Hasselt University, Belgium	
12:30	**Lunch Break & Exhibition**		
13:30 - 15:30	Industrial program Session Chair: **Kim Petersén**, HDC Room: Renen Abstracts-A	Industrial and product program Session Chair: **David Källberg**, FPGAworld Room: Räven Abstracts-A	Product Program Session Chair: **Ove Boström**, FPGAworld Room: Gasellen Abstracts-C
	A5: **Accelerating embedded software development and ASIC verification with FPGAs** Juergen Jaeger, Cadence Design Systems, USA A6: **OpenCL in an Embedded Environment,** Johan Karlsson, Xelmo AB, Sweden, more information A7: **New Low Level C programming book for students with Altera BeMicro 10** Lars Bengtsson, University of Gothenburg, Sweden A8: **The FPGA on a Printed Circuit Board** John Steinar Johnsen, Elmatica AS, Norway (more information)	A9/10 (1 hour): **OSVVM for VHDL Verification** Jim Lewis, SynthWorks Design Inc, USA, more information, Course A11: **The IP-component I2C_Master_IP** Lars Högberg, AGSTU School, Sweden, more information **Product Presentation** C9: **SmartFusion2 – Embedded system "Root-of-Trust" Secure Boot Demonstration** Peter Trott, Microsemi, USA D1, **Tutorial 13:30- 15:00: Universal VHDL Verification Methodology (UVVM)** Room: **Storken,** booking in reception. Espen Tallaksen (Information) Course	C5: **FPGA based CAN FD communication brings CAN to new levels,** Ludvig Vidlid, Synecitve Labs, more information C6/7: (1 hour): **Optimizing HW/SW partition of a complex embedded system using C/C++** Olivier Tremois, EMEAI DSP Specialist FAE, XILINX, USA C8: **Title: Max10 - The next step in low cost FPGA integration** **Presenters:** Nikolay Rognlien, MDE Programmable Logic, Arrow Norway AS, (more information, info_2)
15:30	**Coffee Break & Exhibition, Sponsor** ALTERA		
16:00 - 16:30	Panel Discussion **What will be the impact of Intel on Altera? Any reason to be frightened? Xilinx next?** Session Moderator: Lennart Lindh, FPGAworld Opinion presenter: **Mike Dini**, Dini Group, USA (10 minutes without interruption) Panel: **The participants in the room!** Room: Renen		
16:30	**Go Home Drink in the Exhibition hall**		

Exhibitors and Product Presenters	ÅF, Sweden Aktuel Elektronik, Denmark Elektroniktidningen, Sweden The Dini Group, USA ELMATICA AS, Norway	Exostiv Labs, Belgium Linear Technology, USA Silica, USA XILINX, USA Synective Labs, Sweden	Microsemi , USA Arrow Electronics, USA Altera,USA InnoFour, Netherlands AGSTU AB, Sweden