The gates are open

An overview of the OpenRISC ecosystem

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- Senior Digital Design Engineer at Qamcom
  - Qamcom Research & Technology is a product development and specialist service provider in the areas of signal processing and communication systems, automotive systems and functional safety
- OpenRISC core developer
  - Main developer of FuseSoC
  - Maintainer of many cores and utilities
  - Writes about OpenRISC development

Why Open Source Hardware?

Closed source

I have a closed-source design and...

- ...there seem to be a bug
- ...it has a restrictive license
- ...the documentation is lacking
- ...support is slow
- ...I really want to know how it works

Open source

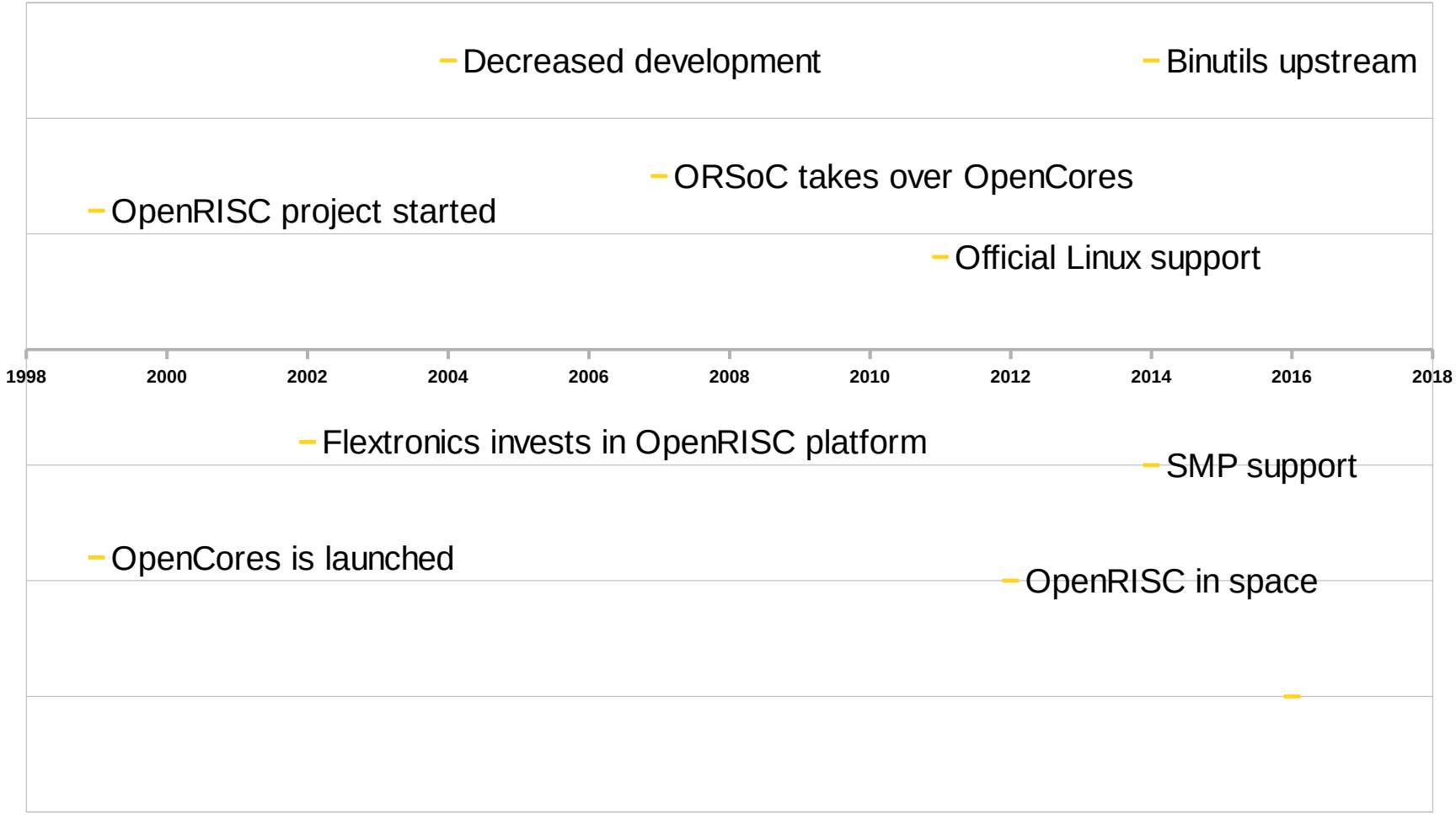
Key benefits

- Minimize end-of-life problems
  - Easier porting to newer technologies
  - Enables re-design without changing the software
- No technology lock-in
  - Gives the upper hand during price negotiations
  - Re-usability

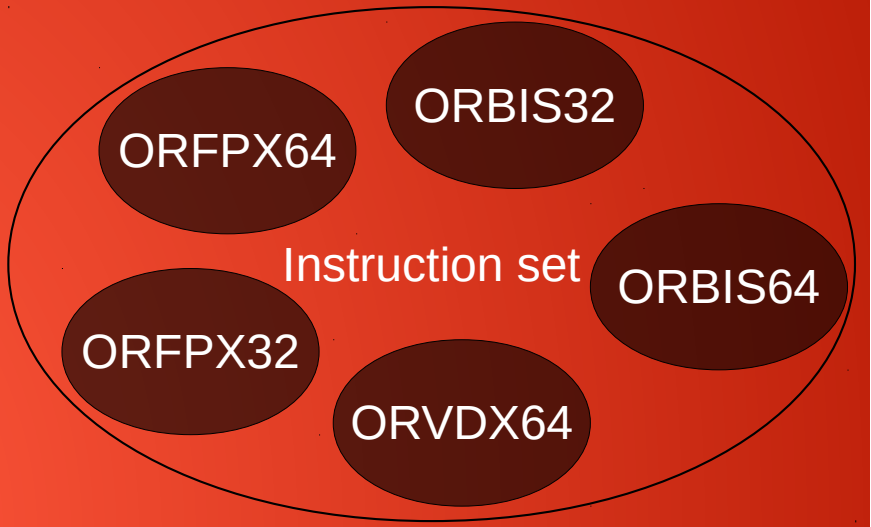
The OpenRISC project

- The aim of the OpenRISC project is to create free and open source computing platforms. The project strives to provide:
  - a free, open source RISC architecture with DSP features
  - a set of free, open source implementations of the architecture
  - a complete set of free, open source software development tools, libraries, operating systems and applications
- Started by Slovenian university students, lead by Damjan Lampret
- The first architecture is the OpenRISC 1000 architecture (or1k),
- first implementations were or1ksim (C) and the OR1200 (Verilog)
- Initiated along with OpenCores, an open source hardware development community

OpenRISC timeline



OpenRISC 1000 architecture



- 32/64-bit load/store RISC
- Inspired by MIPS-I / DLX
- Fixed-length instructions
- Base integer ISA with vector, FP and custom instructions as ISA extensions
- Cache, MMU, PIC, Timer, Debug unit, Power management

OpenRISC 1000 Implementations

- or1200 – The original verilog implementation
- or1ksim – The golden reference C model
- mor1kx – The new and improved verilog implementation
- jor1k – A javascript implementation

These are only the most noteworty. Several more exist

Performance

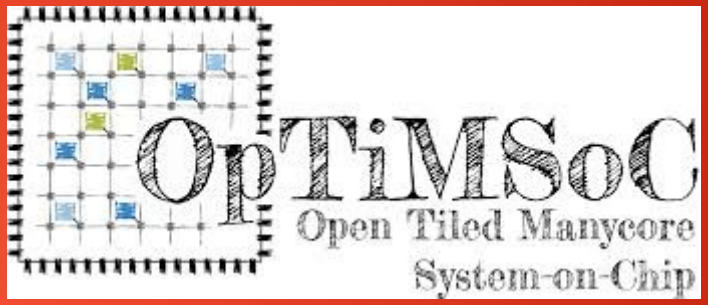
mor1kx

- Coremark 1.66/MHz/core
- Speed
  - ~85MHz Standard configuration on Cyclone IV
  - ~200MHz No caches on Virtex-6

Where is it used?

Academia

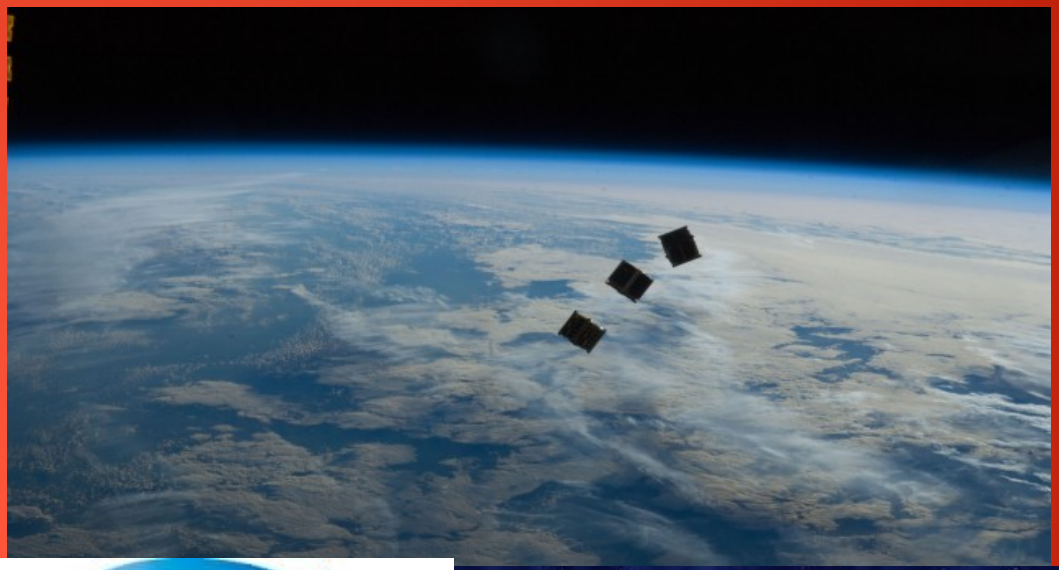
- Research
  - Munich - OpTiMSoC
  - Florida - Branch predictors
- Education
  - Munich
  - Lisboa
  - Linköping
  - New Mexico
  - Texas
  - Mechelen
  - Cambridge



Where is it used?

Industry

- FPGA/ASIC
  - NASA TechEdSat
  - Samsung DTV
  - Allwinner SoC
  - Zigbee ASIC
  - ...many more under NDA...
- EDA reference workflow
  - UVM
  - CVC

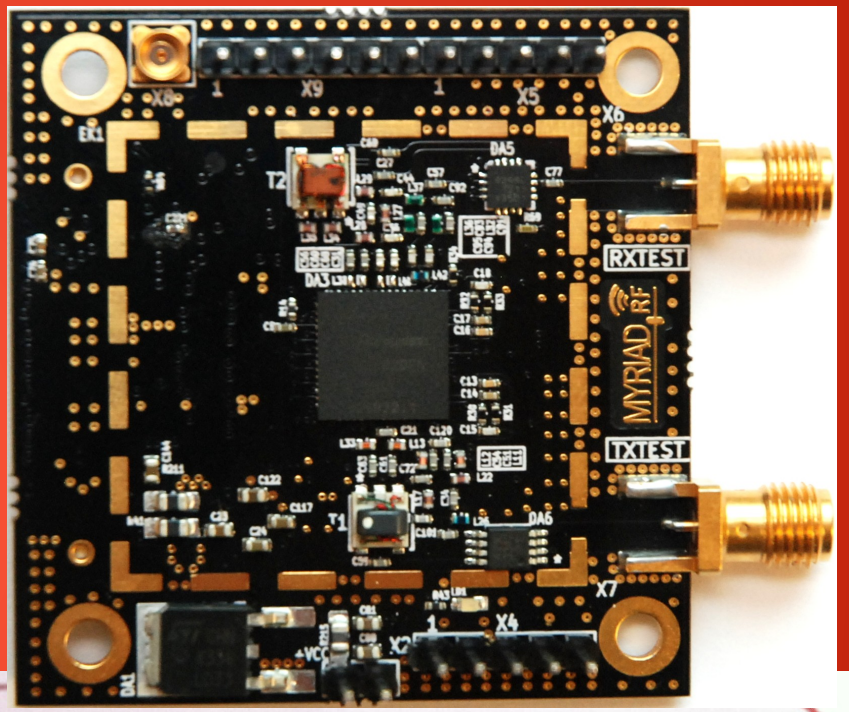


UVM

Where is it used?

Hobbyist

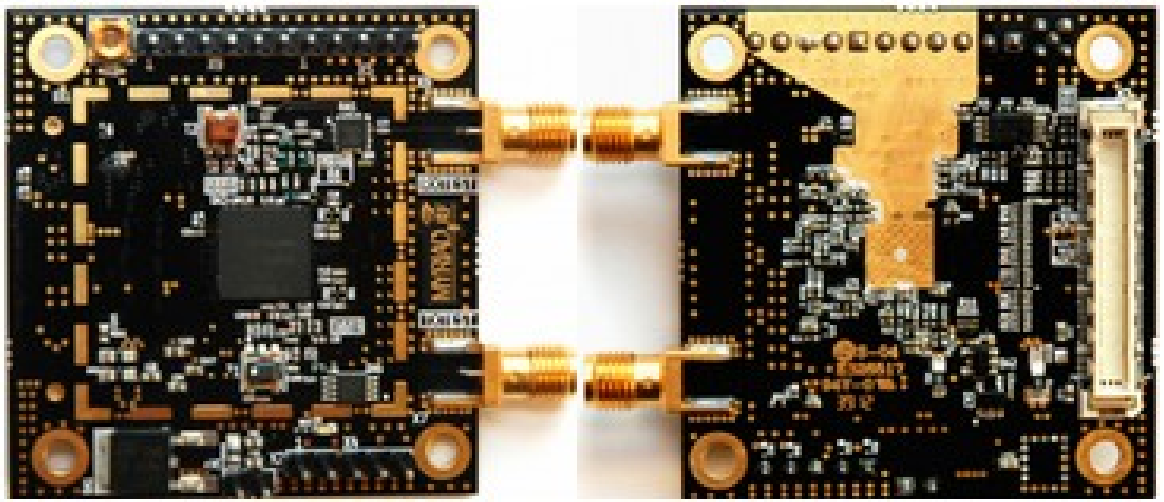
- Learning and tinkering
- Platform for projects
  - Bus Pirate
  - Arduissimo
  - MyriadRF



MyriadRF Board (LMS6002D)

- **MyriadRF – a low cost universal radio platform, based on LMS6002D FPRF transceiver (http://myriadrf.org/)**

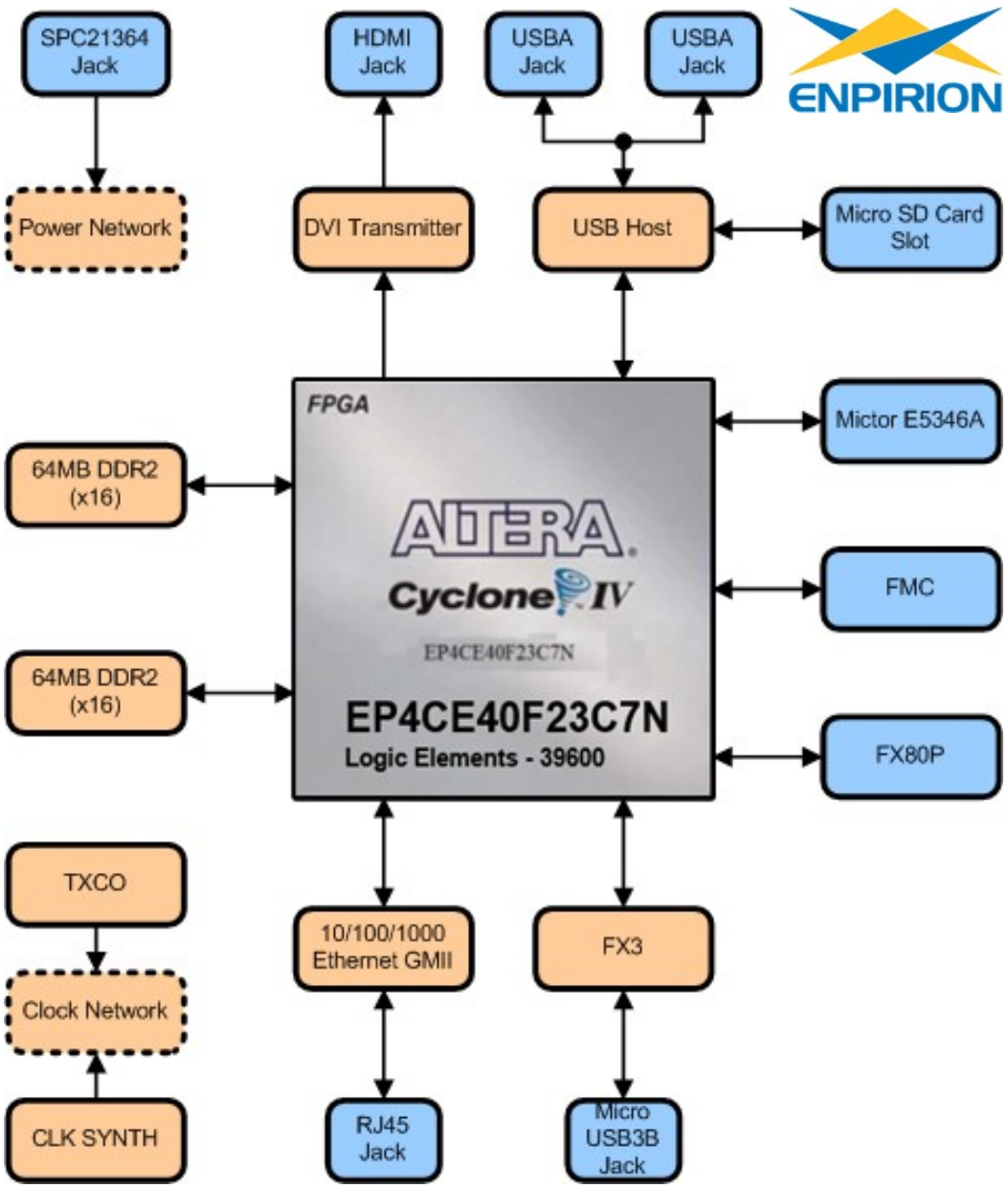
- **It enables developers to implement their products for a wide variety of wireless communication systems by having:**
  - A ready-made design and implementation to accelerate development time.
  - A wide community support through the Open Source database.
    - Boards
    - Projects
    - Software
    - Forum



- **Community support**
- **Purchase through DigiKey**

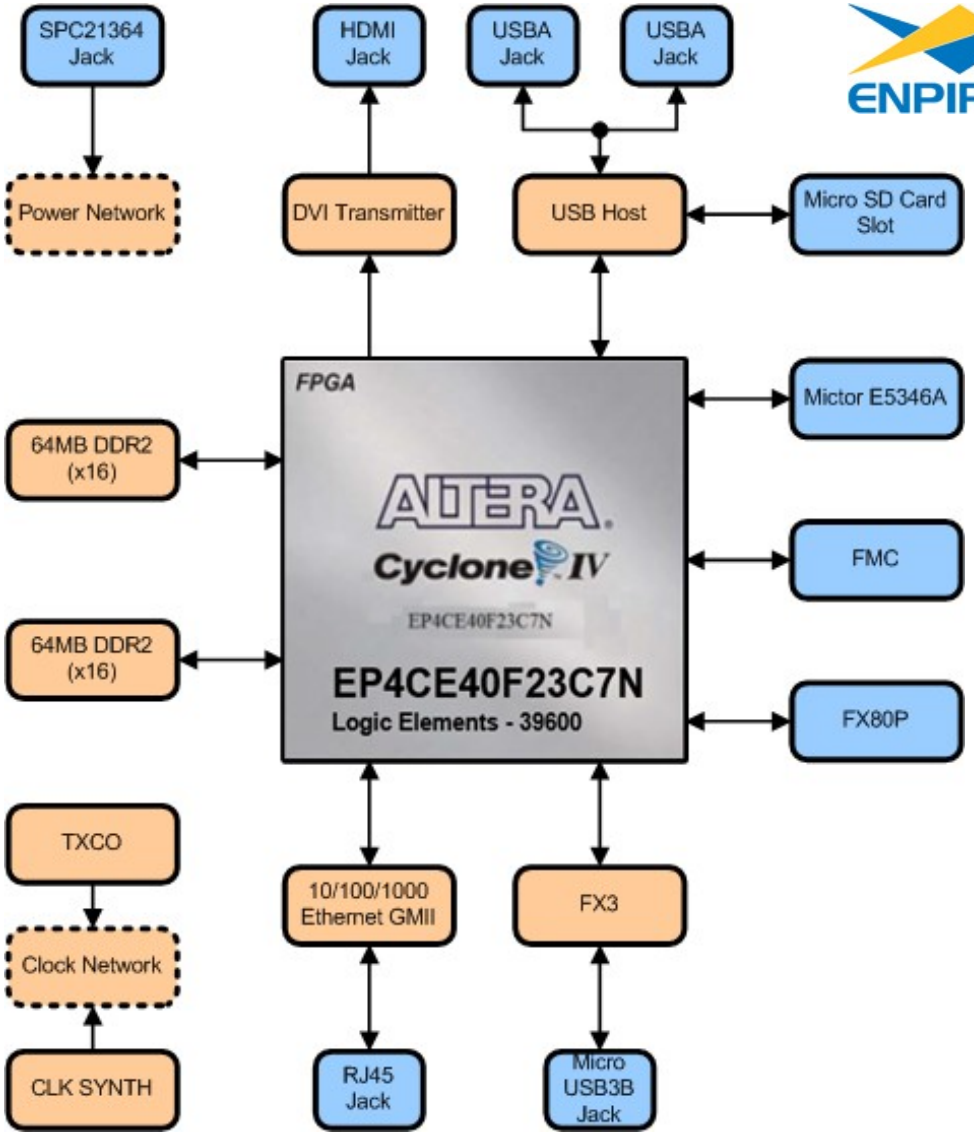
price of $299 US dollars

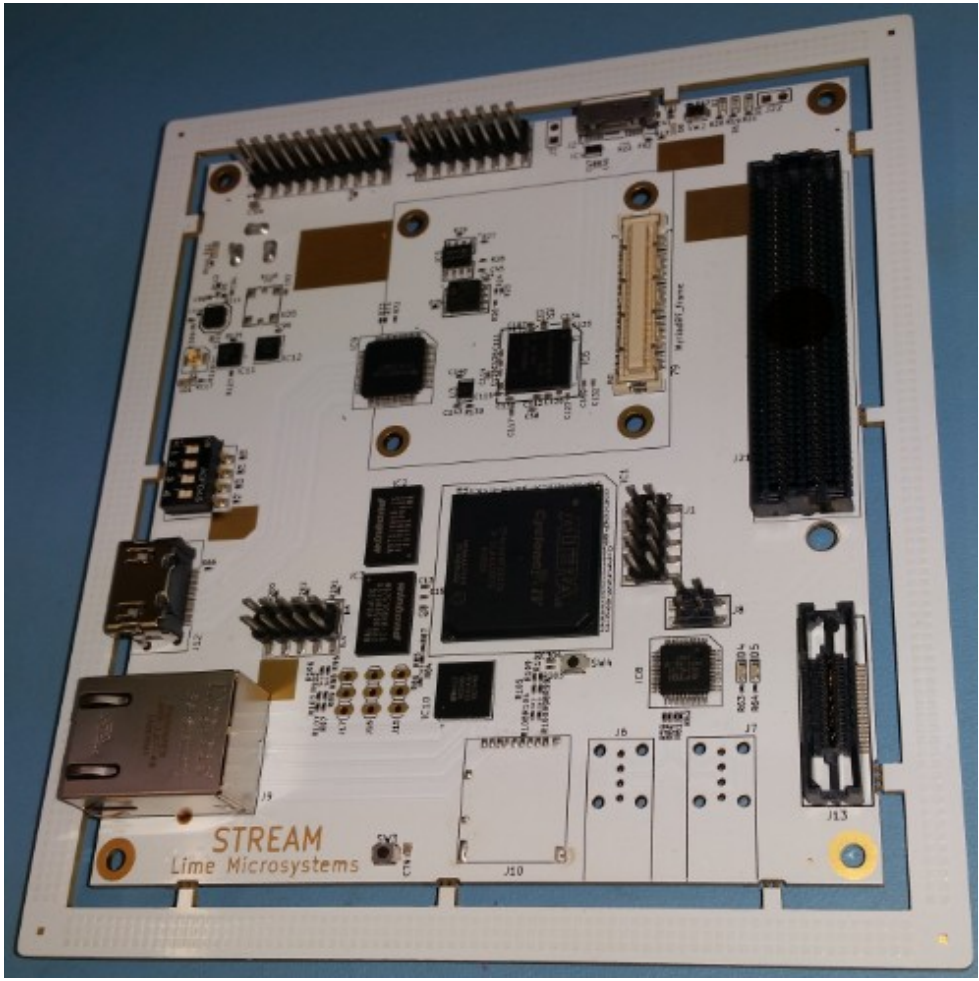
Altera based Wireless platform
Block Diagram Stream board



- Completely Open Source
- Runs all the RF related functions
- Softcores for FPGA[LINK]
- Runs Lime FFT viewer
- Connects to Agilent test equipment
- Connects to all the Lime evaluation kits

Lime Altera based Wireless platform
Connects to all MyriadRF boards





“A CPU is only as good as its peripherals and software”

O. Kindgren, 2014

Hardware support

- Wishbone is the preferred bus standard
  - Royalty-free
  - Large set of IP from commercial vendors, CERN, OpenCores and others
  - Utilities such as interconnect generators, bridges to other buses and BFMs are available in several languages
  - Burst modes, low overhead

Hardware support

Peripheral controllers

- I2C, AC97, Ethernet, ATA, SPI, DVI, UART, SDRAM, USB, JTAG and many more

Available board ports

- DE0 Nano, Atlys, ordb1, LX9 Microboard, DE1, SoCKit, NEEK, ordb2a, ML501

FuseSoC

FuseSoC is a SoC framework designed to increase re-use and decrease development time

- Handles dependencies between IP cores
- Provides a unified interface for different EDA tools
- Supports block-level and system-level simulations
- Currently support for
  - building with Quartus and ISE (Diamond is in the works)
  - Simulating with Icarus, Modelsim and Verilator (CVC and Riviera is in the works)

Software support

- Development tools
  - GNU Toolchain (GCC + Binutils)
  - LLVM
  - OpenOCD
  - uBoot/Barebox
- Operating systems
  - Linux
  - RTEMS
  - eCOS
  - uCos II
  - (NetBSD is in the works)
- C Libraries
  - musl
  - glibc
  - uClibc
  - newlib
-


Monkey Island 2: LeChuck's Revenge (DOS/English)
You do turn up in the strangest places.

Contact

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