FPGAworld 2014

# SimXMD: Simulation-based HW/SW Co-Debugging for FPGA Embedded Systems

Ruediger Willenberg and Paul Chow

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# "Women and Men can never be friends.



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# "Designers and Tools can never be friends.



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# "Designers and Tools can never be friends. The Sex will always get in the way."



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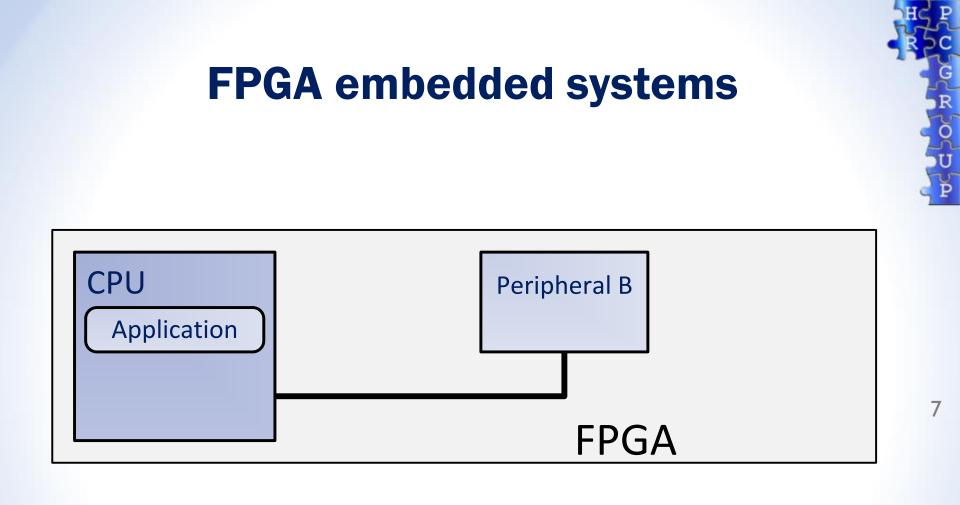
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# "Designers and Tools can never be friends. The Semantics will always get in the way."

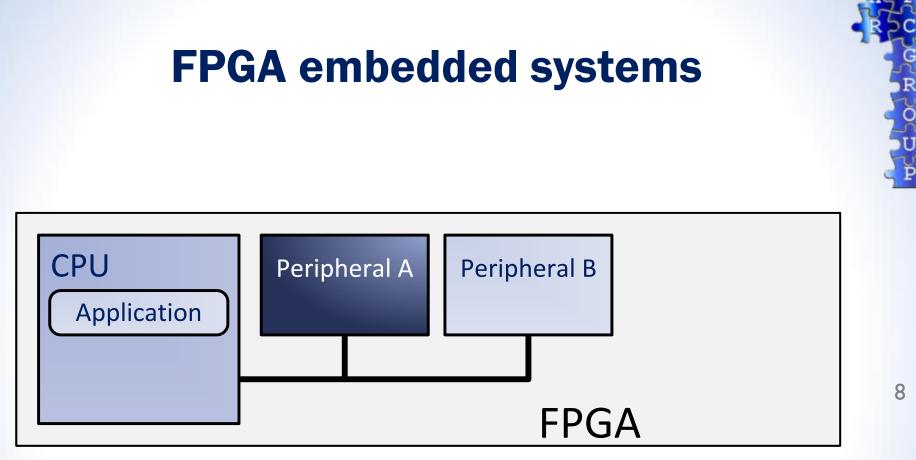


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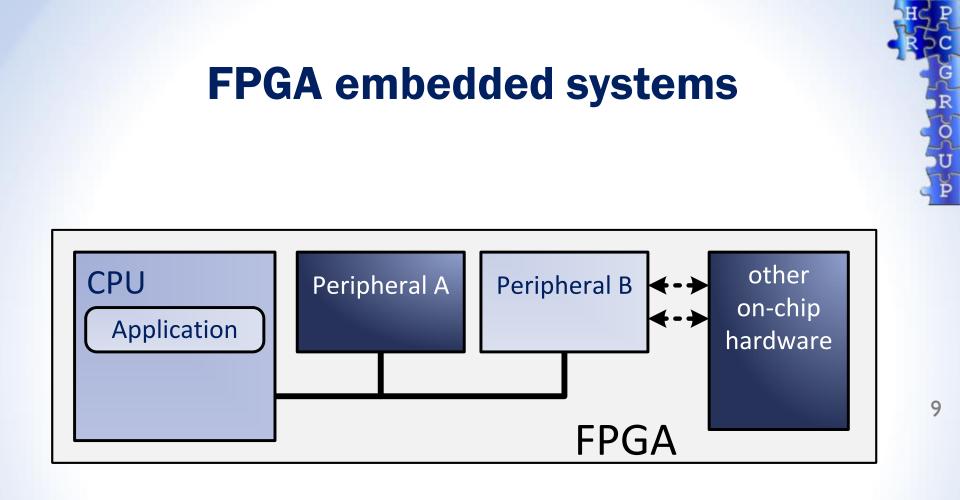
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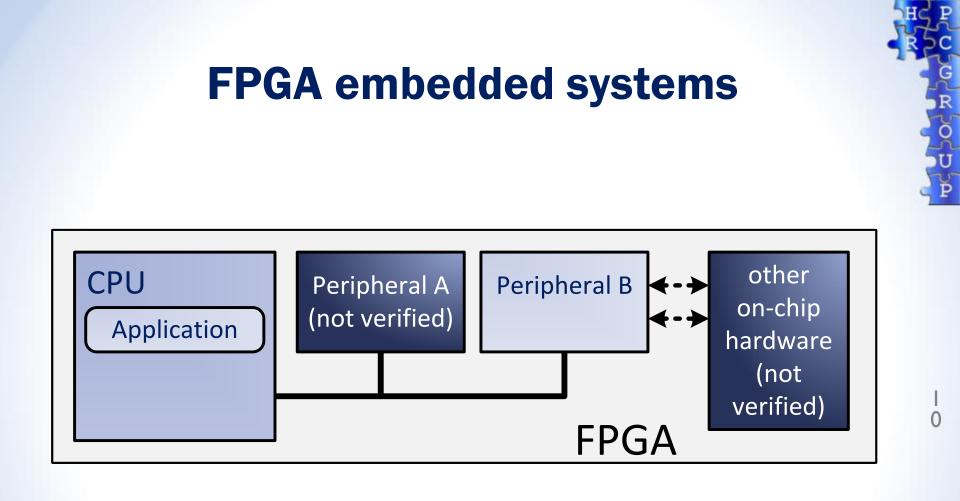




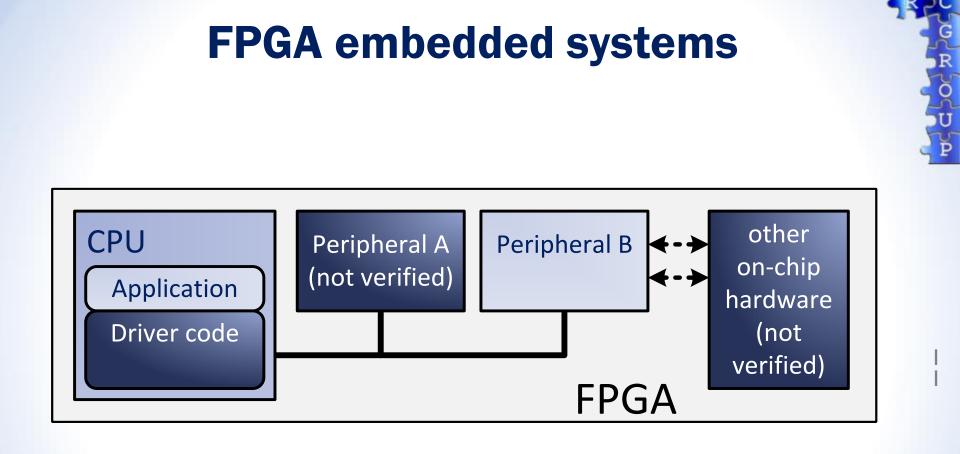




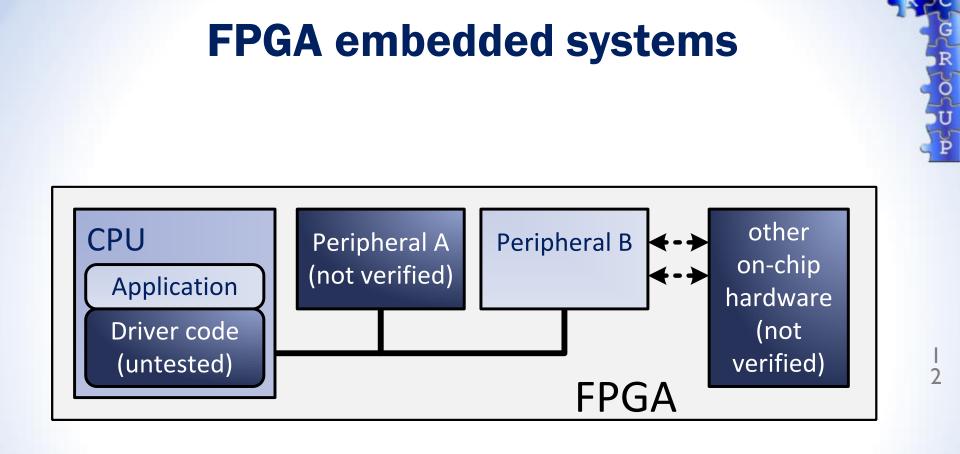




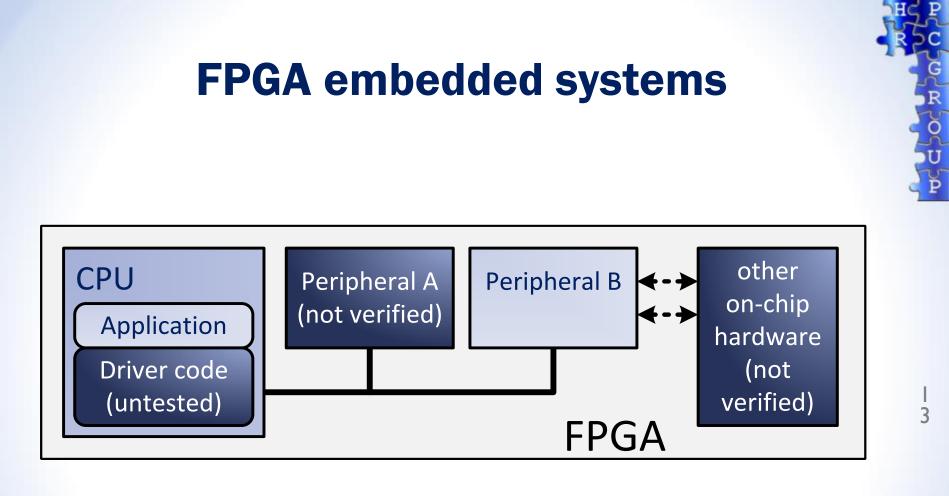








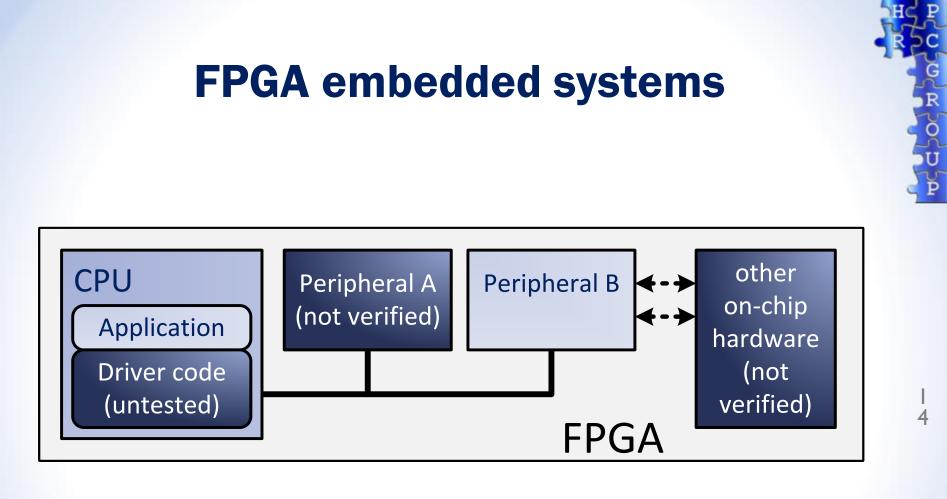




Optimal: Debug hardware, software and their interaction together



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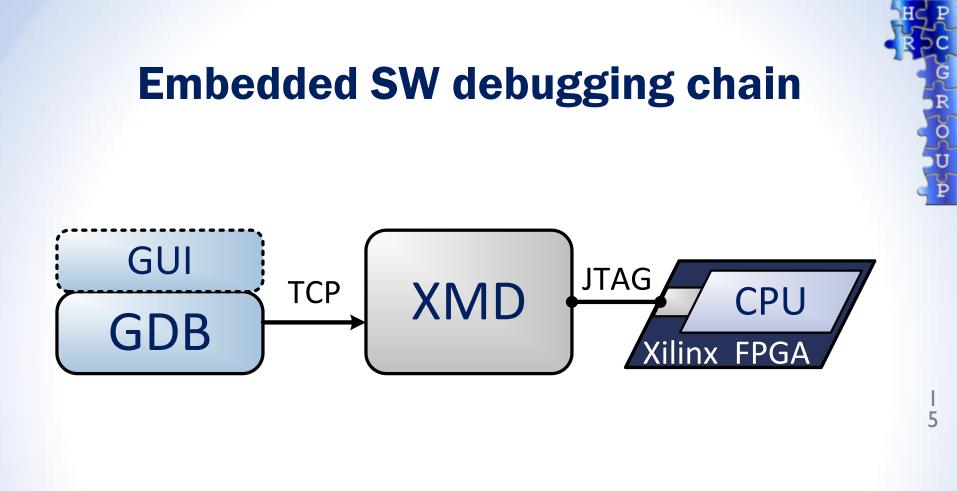


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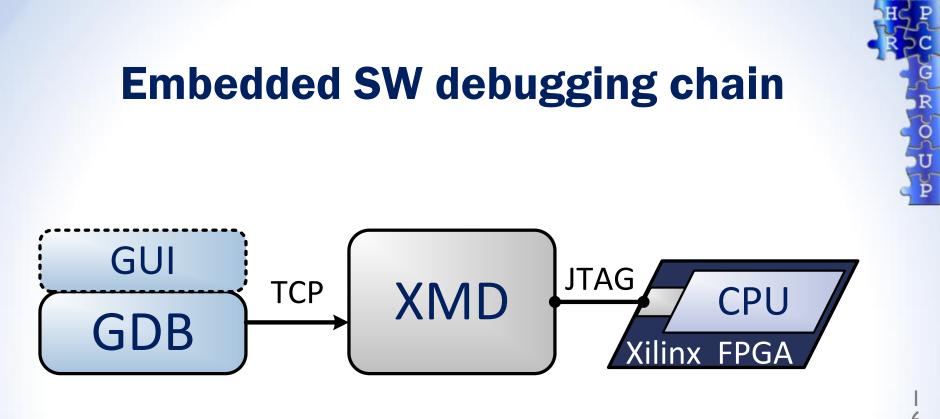


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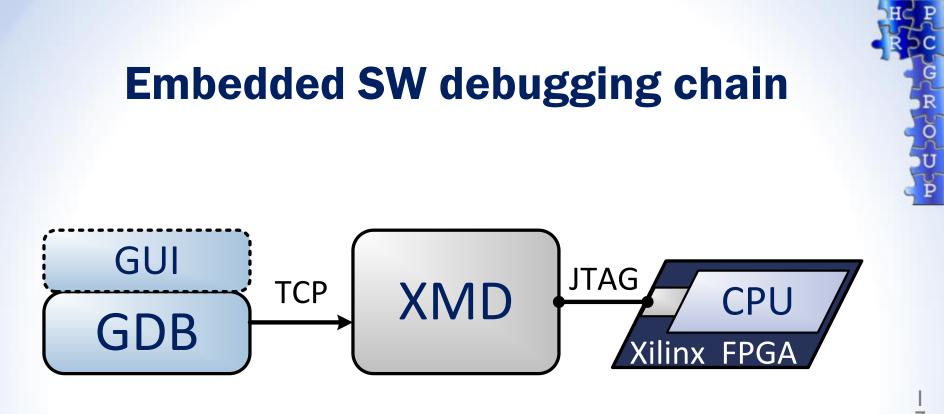






Debugger on host system



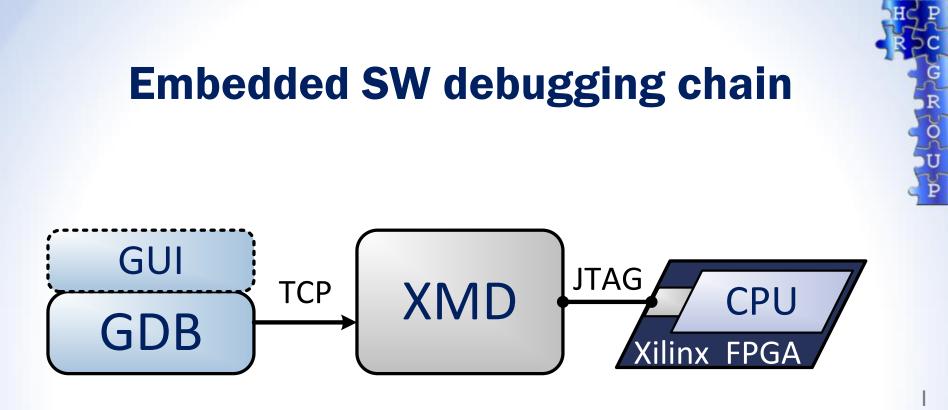


• Debugger on host system

• Software runs on target system

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- Debugger on host system
- Vendor-specific interface software
- Software runs on target system

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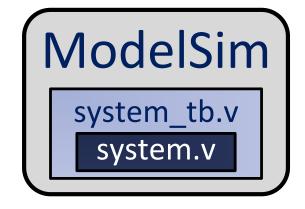
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#### **Embedded SW debugging chain**

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Debug 🕄		🕨 00 📕 🎝 🕽	🗠 .e 🗟 🖬 🛠 🕻		network_nv_test.c 🕱
C SimXMD_microblaze_0 [C/C++ Application]					<pre>#include "xparameters.h" #/plude "xparameters.h"</pre>
🕶 🔐 gdb/mi (9/8/14 1:04 AM) (Suspended)					<pre>#include "stdio.h" #include "fsl.h"</pre>
👻 🔊 Thread [1] (Suspended: Breakpoint hit.)					#include "tst.h" #include "xgpio.h"
	etwork_rx_test.c:49 0x0000				winclude xgpio.n
/home/willenbe/bin/Xilinx/14.1/ISE_DS/EDK/gnu/microblaze/lin64/bin/mb-gdb (9/8/14 1:04 AM)					#define PACKET SIZE 4
📕 /home/willenbe/Projects/SimXMD_Demo_v14/SDK/network_rx_test/Debug/network_rx_test.elf (9/8/				elf (9/8/	#define MAX PACKETS 256
				F	
v= Variables 🛙	- 1	Registers 🕄	🔬 🍕 📄 🕯	~	<pre>void read_network_packet(unsigned int* packet);</pre>
		7 Name	Value	121	<pre>void decrypt_packet(unsigned int key, unsigned int* packet, unsigned int* buffer);</pre>
	≌ •4 ⊟   \$* • • •8		Value	F	
Name	Value	1919 rO	0		<pre>unsigned int cryptokey = 0xDDCCBBAA; // global: not re-initialized on reset unsigned int my packet[DACKET_SIZE];</pre>
00- packet_cnt	5	1919 r1	0x00008040		<pre>unsigned int rx_packet[PACKET_SIZE]; unsigned int rx_packet decrypted[PACKET_SIZE];</pre>
😑 rx_buffer	0x00008068	1919 12	3842		XGpio LEDs;
🔸 👄 buffer_ptr	0x000080b8	1911 r3	32952		Adpio EEDS,
00- t	4	1919 r4	3		int main (void)
		1918 15	4184		
		1919 r6	8		//unsigned int cryptokey = 0xDDCCBBAA; // local: re-initialized on reset
		1919 r7	57		
		1919 r8	0		<pre>unsigned int packet_cnt = 0;</pre>
		1919 r9	0		<pre>unsigned int rx_buffer[PACKET_SIZE * MAX_PACKETS];</pre>
		1010 -1 0	0	•	<pre>unsigned int *buffer_ptr = rx_buffer;</pre>
Memory 23		T.P.	· 🖬 🔢 🐝 - 1		unsigned int t;
	M (20000 - 20000 - 414				XGpio Initialize(&LEDs, XPAR LEDS DEVICE ID);
				1.4	XGpio SetDataDirection(6LEDs, 1, 0x0);
0x8068	Address 0 - 3	4 - 7 8		1-1	
	00008060 B8800				<pre>while(packet_cnt &lt; MAX_PACKETS)</pre>
	00008070 28000		0000000 0000000		
	00008080 2E000	000 2F000000 3	0000000 31000000		
	00008090 00000	000 32000000 3	3000000 34000000		🗟 Console 🛿 🕹 🔂 🔝 🖬 🖬 🖓
	000080A0 35000	000 0000000 3	3700000 3700000		C-Build [network_nz_test]
	00008080 38000	000 39000000 0	0000000 0000000		elfcheck network_rx_test.elf -hw//SimXMD_Demo_v14_hw_platform/system.xml -pe microblaze_O  tee "network rx test.elf.elfcheck"
	000080C0 00000	000 0000000 000	0000000 0000000		"network_rx_test.elt.eltcneck" elfcheck
	00000 00080000	000 0000000 000	0000000 0000000		Xilinx EDK 14.1 Build EDK_P.15xf
	000080E0 00000	000 0000000 000	0000000 0000000		Copyright (c) 1995-2012 Xilinx, Inc. All rights reserved.
	00008050 00000	000 0000000 0	0000000 00000000	<b>*</b>	Command Line: elfcheck -bw / /SimXMD Demo v14 bw nlatform/system xml -ne



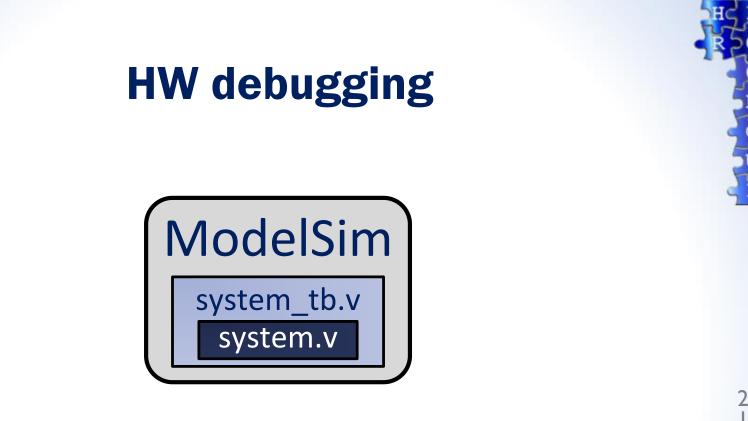
#### **HW debugging**





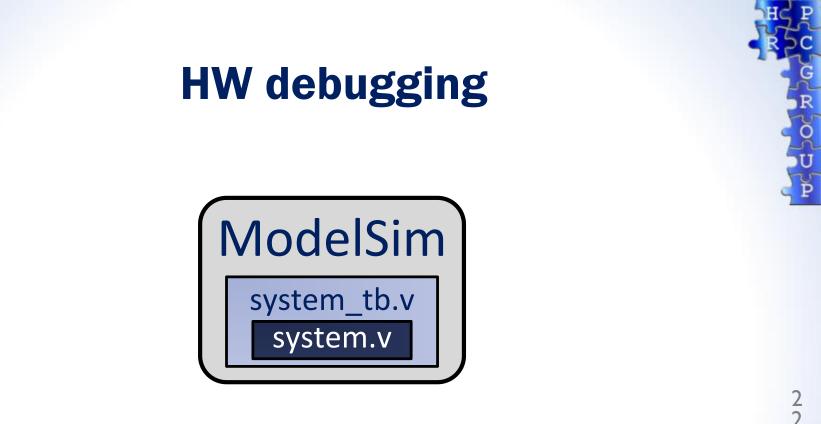
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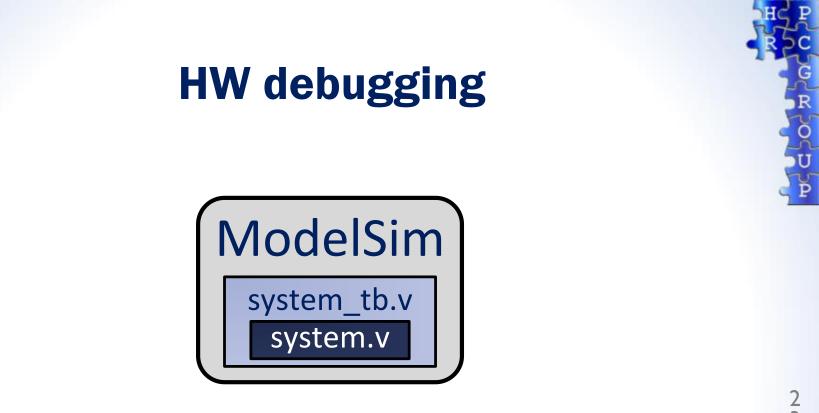
• Cycle-accurate digital simulator





- Cycle-accurate digital simulator
- A system model in HDL

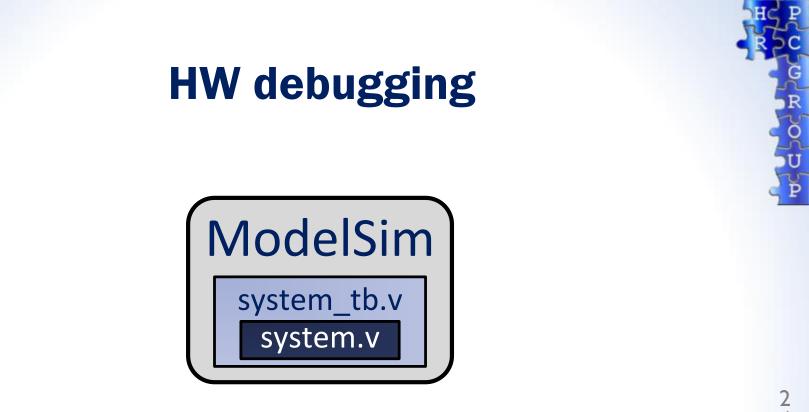




- Cycle-accurate digital simulator
- A system model in HDL
- Testbench instantiates and stimulates model



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- Cycle-accurate digital simulator
- A system model in HDL
- Testbench instantiates and stimulates model
- All internal signals observable

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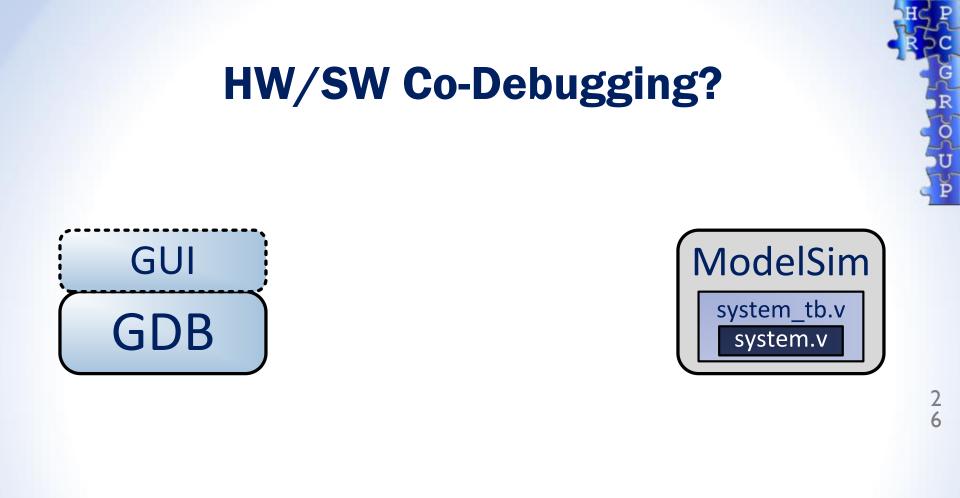


# **HW debugging**

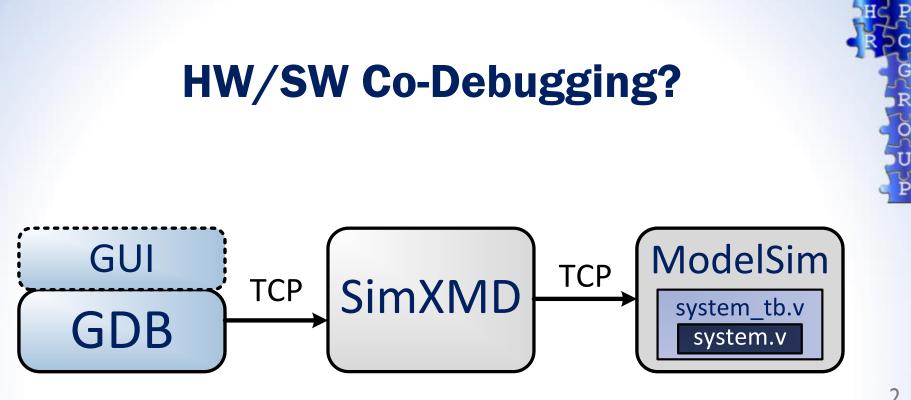
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- <b>2</b>	Msgs	
	(DEBUG microblaze)	
processor_rst		
instructions		
Trace_PC	0000021c 0.000.0000000000000000000000000000000	
Trace_Valid_Instr	3021 efd4	
- A Memory access	(Memory access)	
• Trace_Data_Byte_Enable	0001 X X0001 X1111 X X1111 X X0 X X X0001 X X1111 X X0 X1111 X X0001 X X0001	
🛃 🚽 Trace_Data_Write_Value	6c6c6c6c <mark>// /0000 // /0 /000000 /000/ /4 / // /0000 // //0000 // //000/4 /000/ /6 /9/ // /0</mark>	
💽 🕂 🕂 Trace_Data_Address	00008040 <mark>]                                    </mark>	
Trace_Data_Read		
E 🔶 Registers	(Registers)	
Trace_Reg_Write		
Trace_Reg_Addr		
Trace_New_Reg_Value	00008040 <u>X X000¢ X X X X000000 X X X0 X X0 X X0 X X0 X X X X</u>	
	00000000 0000908c <u>00000000 0000000 0009048 00 000000000 00000000 0000900</u>	
	49 48	
• oncryption_key	decdbcab	
🖃 🤣 network_rx_Data_pin	decdbc9a.decdbc9b	
network_rx_Valid_pin	sto	
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fsl_network_read		
1400	3477500 ps 3200000 ps 3200000 ps 3400000 ps	



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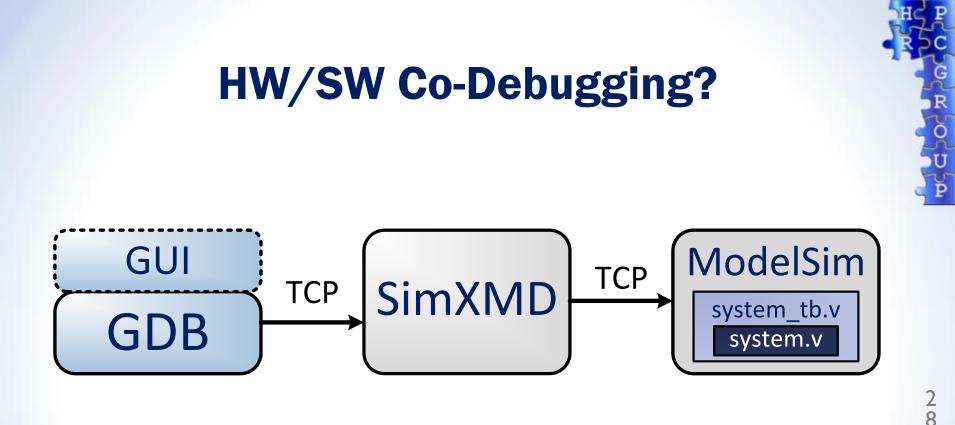






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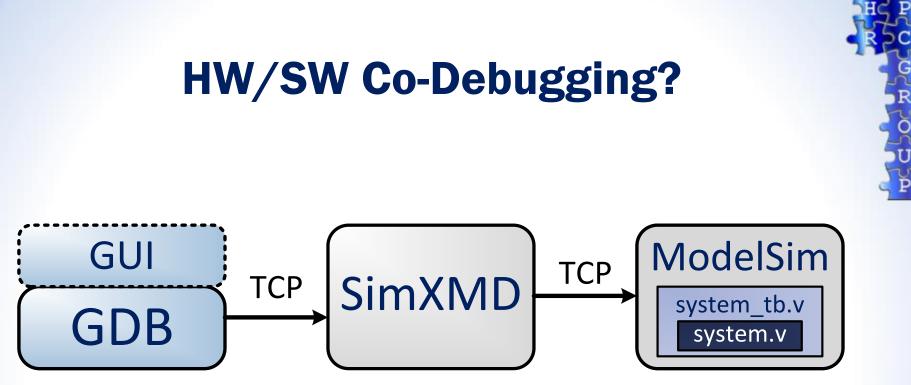


SimXMD: Simulation-based eXperimental
 Microprocessor Debugger



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- SimXMD: Simulation-based eXperimental
   Microprocessor Debugger
- Translates debugger requests into simulator commands

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# **Key SimXMD enablers**

- GDB Remote Serial Protocol
  - Defines requests and replies for:
    - Setting/deleting breakpoints
    - Advancing execution by instruction, line, breakpoint
    - Reading registers or memory state



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- ModelSim (Tcl) TCP server capability
  - Can receive remote commands and send back results

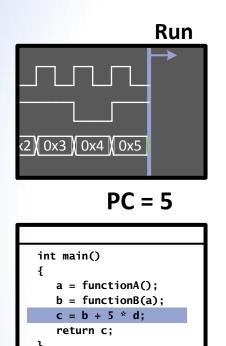


# **Operating SimXMD: Preparation**

- I. Simulation model generation by design tool
   Currently: Xilinx Platform Studio
- 2. SimXMD is started (background operation)
  - Examines embedded project information
  - Modifies simulation model for Co-Debugging
- 3. Compilation of simulation model
- 4. Start of simulation
- 5. Start of preferred debugger (GUI)
- 6. Debugging at will



# **Operating SimXMD: Modes**

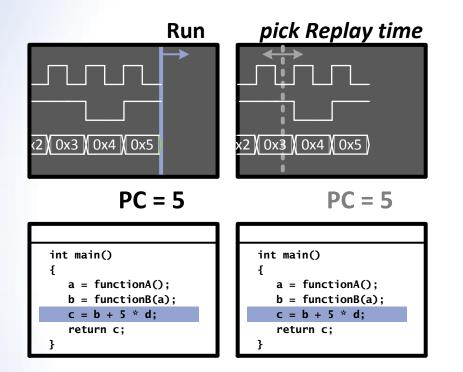


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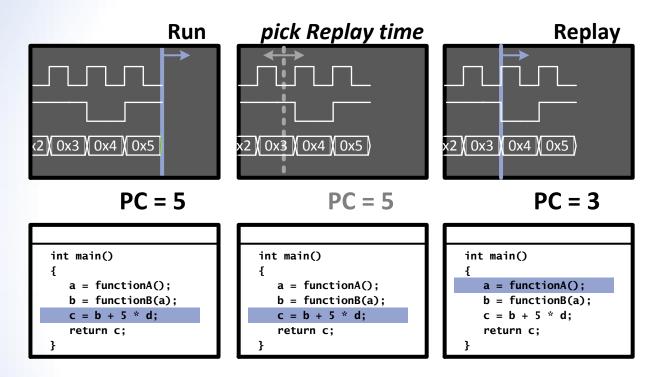


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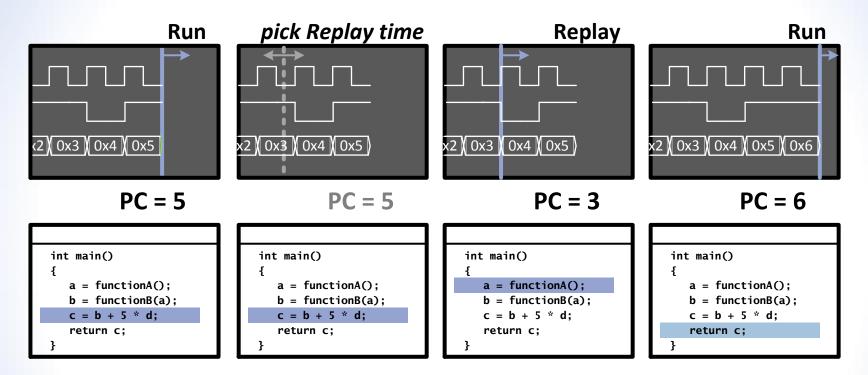
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## **Operating SimXMD: Modes**



- In Run mode, debugging drives the simulation
- In Replay mode, debugging iterates over previously simulated data

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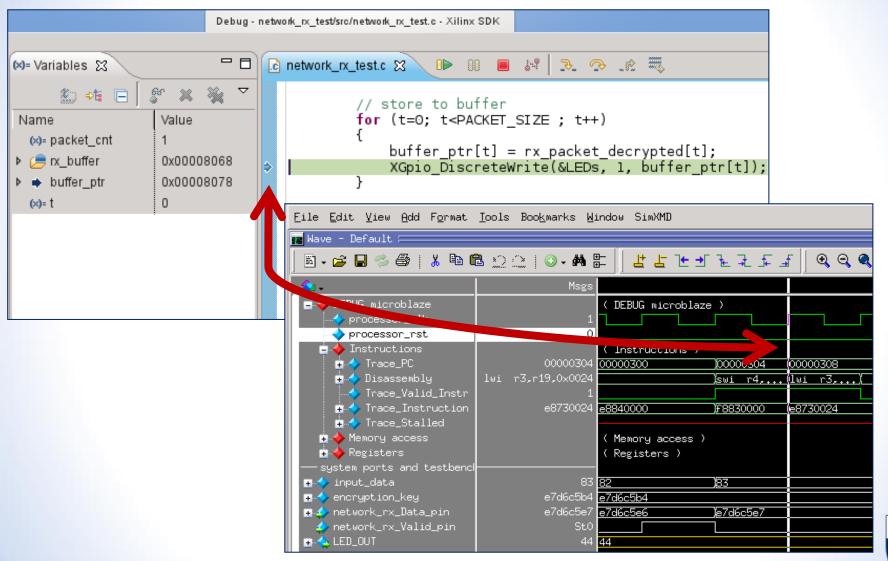


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#### SimXMD at work



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#### **Implementation: Debugging memory**

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### **Implementation: Debugging memory**

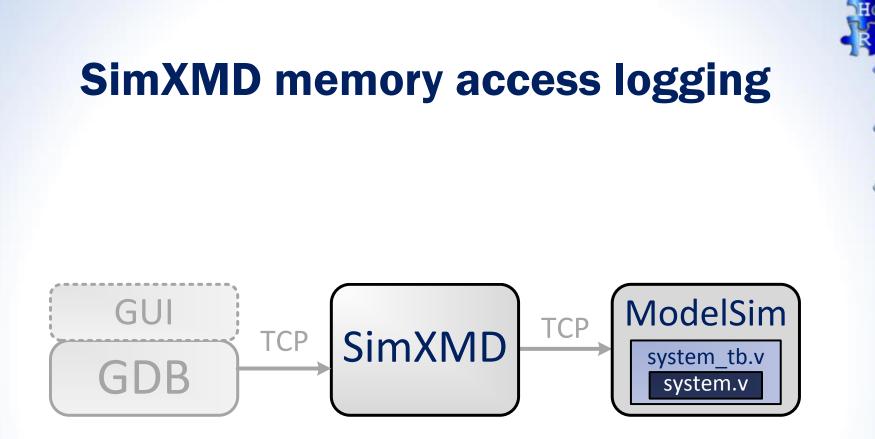
- Digital hardware simulation models the complete memory hierarchy:
  - On-chip and external memory
  - All cache levels
  - Memory-mapped peripherals

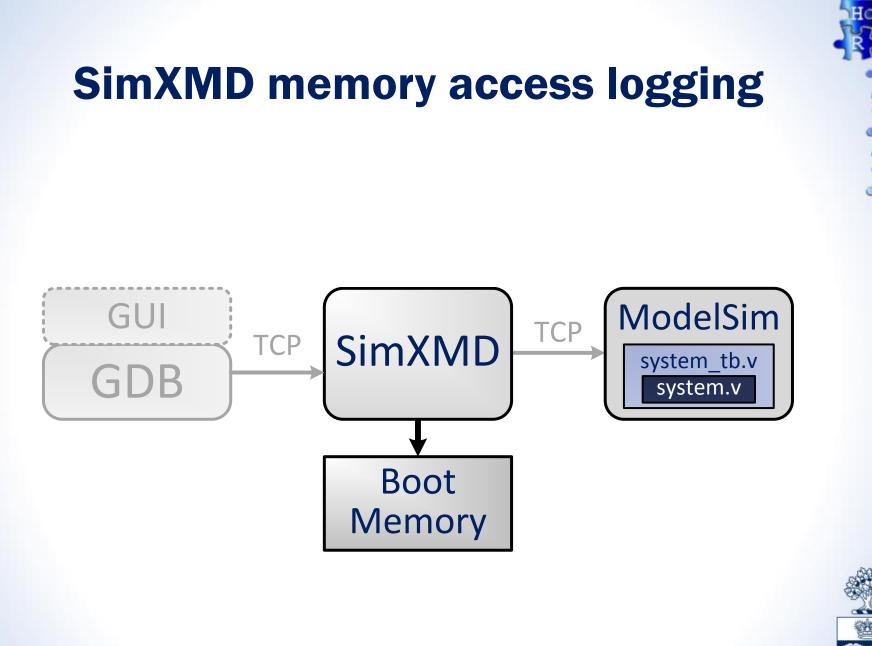


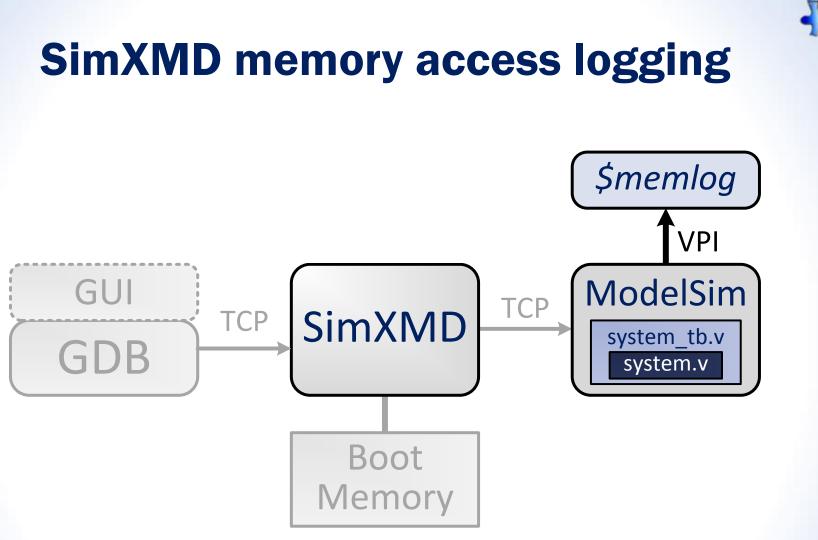
# **Implementation: Debugging memory**

- Digital hardware simulation models the complete memory hierarchy:
  - On-chip and external memory
  - All cache levels
  - Memory-mapped peripherals
- Software debugging uses a flat, linear memory model:
  - The debugger requests a (virtual) memory address
  - The target hardware determines and reads the physical location

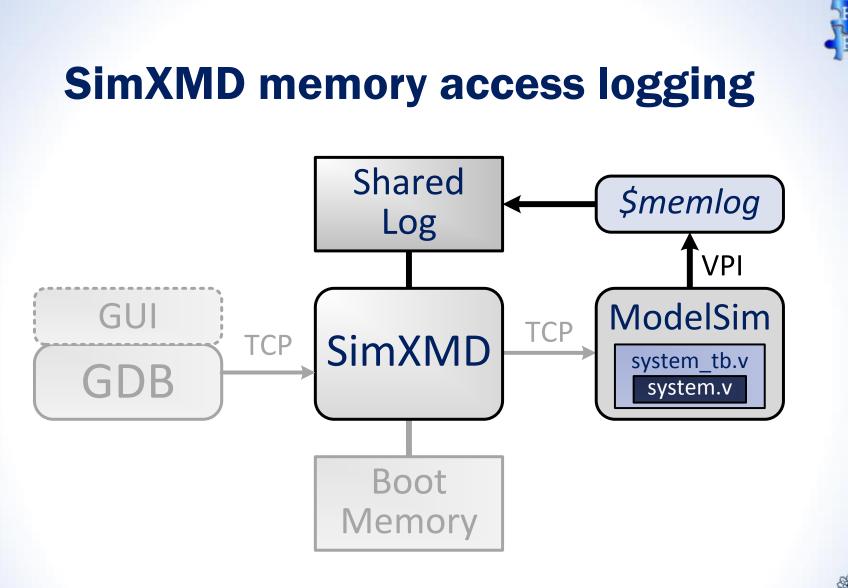






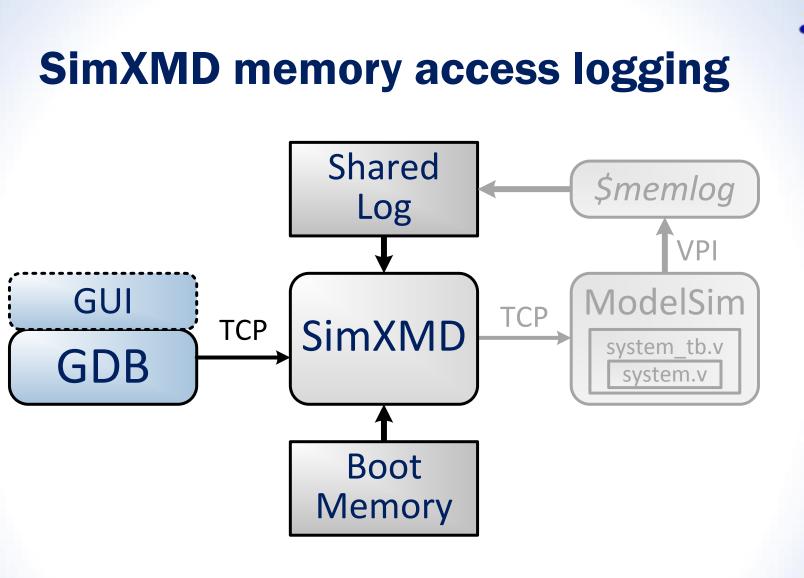


#### VPI:Verilog Procedural Interface



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### SimXMD tool support

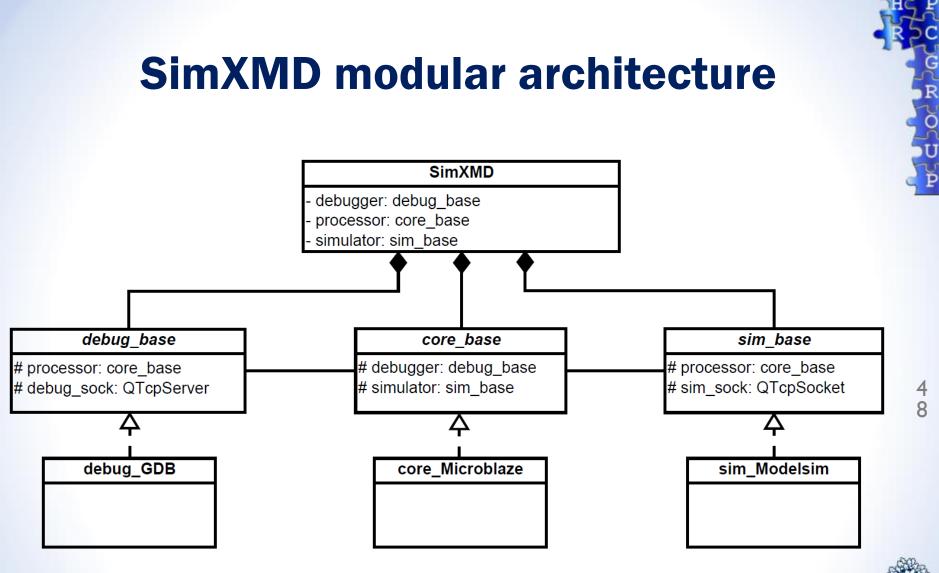
Xilinx Embedded Development Kit >= I3.x

- Xilinx MicroBlaze Processor >= 8.x

- MentorGraphics ModelSim >= 6.6g
- Linux Operating System
- Debuggers
  - Command-line GDB
  - Xilinx SDK (Eclipse)
  - DDD
  - KDbg
  - Nemiver

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Debugger can't modify variables, registers



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- Volatile memory locations might be inaccurate
  - Shared-memory multiprocessing
  - DMA, Busmastering
  - Memory-mapped peripherals



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- Trace Port reports actions after instruction completes; several cycles difference
- Not all MicroBlaze special registers reported
- Instruction code only from on-chip RAM



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Any one core in a multicore system can be selected for debugging



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- Future work:
  - On-the-fly switching between cores
  - Concurrent debugging of several cores



- Any one core in a multicore system can be selected for debugging
- Future work:
  - On-the-fly switching between cores
  - Concurrent debugging of several cores
- The same memory volatility issues apply:
  - Logging of virtual memory accesses per processor
    - Different virtual addresses same physical address?
  - Race conditions likely



### **SimXMD Performance**

 How much do the SimXMD modifications slow down simulation?



# **SimXMD Performance**

- How much do the SimXMD modifications slow down simulation?
- How slow is SimXMD debugging in comparison with debugging a real target?



# **SimXMD Performance**

- How much do the SimXMD modifications slow down simulation?
- How slow is SimXMD debugging in comparison with debugging a real target?
- Test system:
  - Host: Intel i5 Nehalem 4-core, 2.5Ghz, I2GB RAM
  - Target: Xilinx Spartan 6 (Atlys board), JTAG
     Microblaze @ 100MHz, 64kB on-chip BRAM
     AXI bus, one GPIO peripheral

- Application: Writing 32kB byte-by-byte into BRAM



#### **SimXMD** overhead

Write size	w/o SimXMD	w/ SimXMD
l kByte	6.9 s	7.3 s
2 kByte	13.8 s	14.5 s
4 kByte	27.3 s	29.0 s
8 kByte	54.9 s	57.7 s
l6 kByte	109.0 s	7.  s
32 kByte	218.9 s	231.7 s



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# Average overhead: 6.0%



# SimXMD debugging speed

- Same system and application
- Let GDB execute script of 50 "steps" (I code line)
- Average time for a single code step:

Hardware with JTAG	1.350 s
SimXMD Run mode	0.850 s
SimXMD Replay mode	0.313 s





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  - Simultaneous debugging of software and hardware
  - Hardware debugging "timed" by software sections
  - Software debugging without existing/implemented HW



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  - Hardware debugging "timed" by software sections
  - Software debugging without existing/implemented HW
- SimXMD does not significantly slow down reasonable debugging efforts
- SimXMD is open source
- SimXMD's modular architecture facilitates extension to other processors and tools





#### SimXMD can be downloaded at:

#### http://www.eecg.toronto.edu/~willenbe/simxmd





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# Thank you for your attention! Questions?



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