

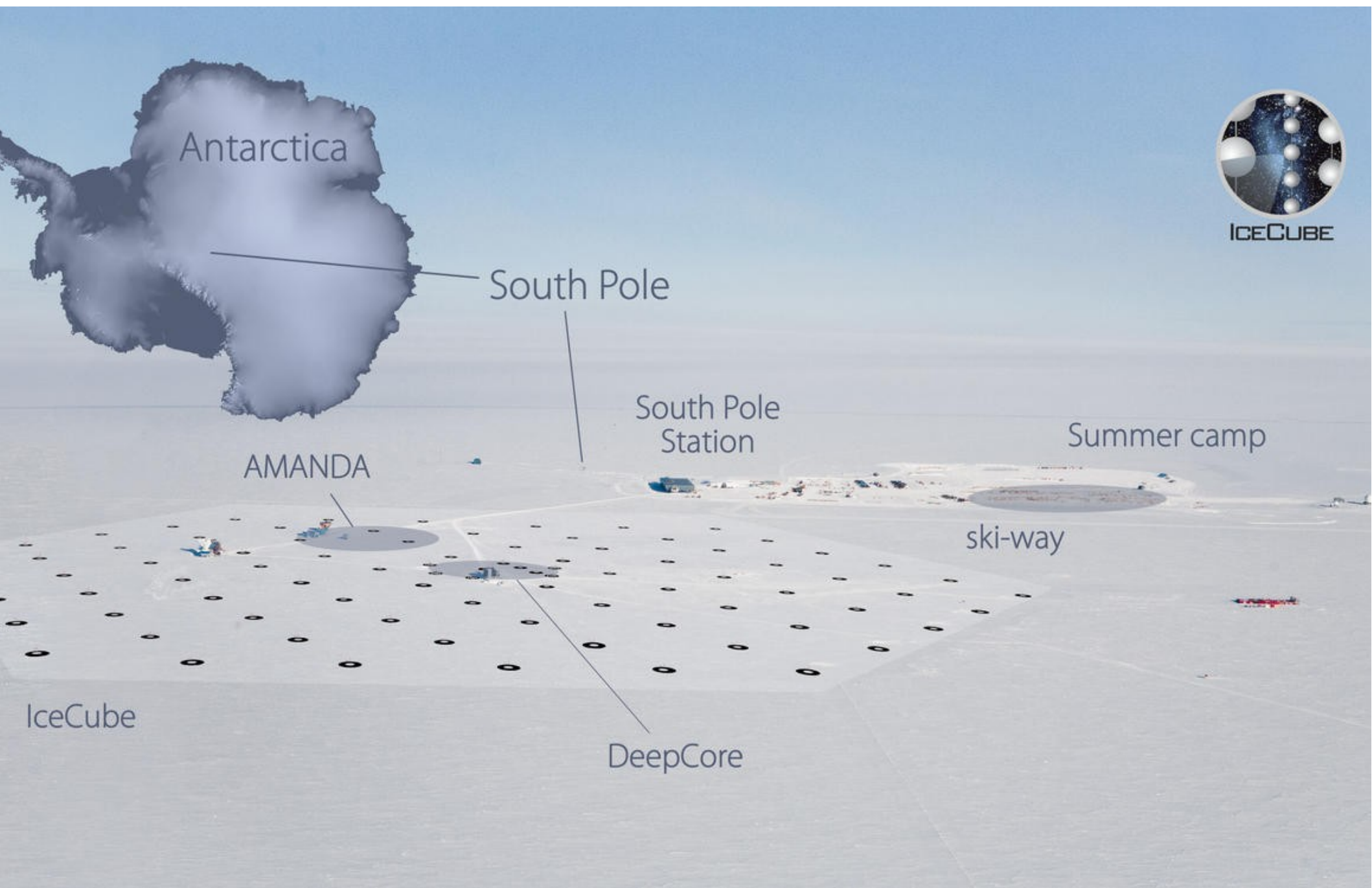
The Track Engine – an FPGA Implementation of a Track-finding Algorithm for the IceCube Neutrino Telescope

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Stockholm University

FPGAworld 2014, Stockholm





Antarctica

South Pole

South Pole
Station

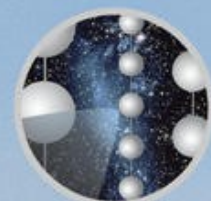
Summer camp

ski-way

AMANDA

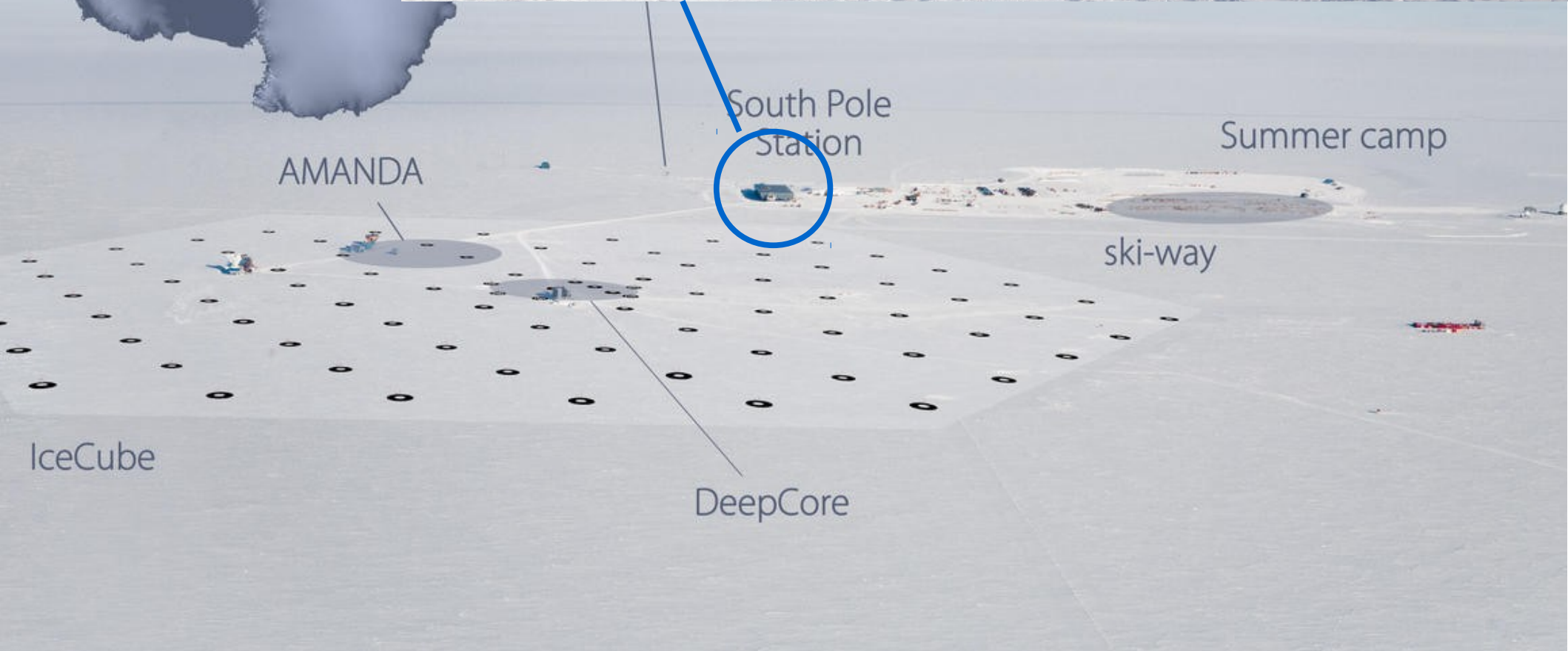
IceCube

DeepCore

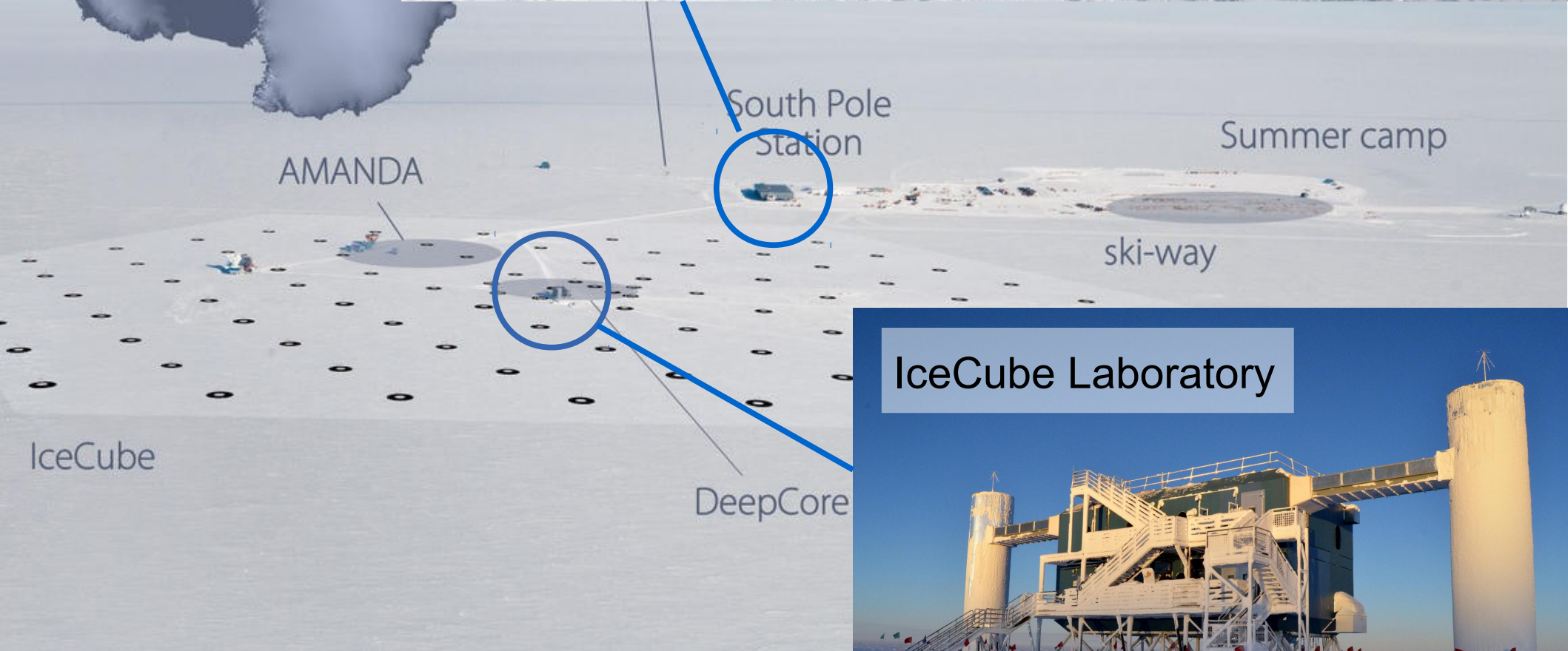


ICECUBE

South Pole Station

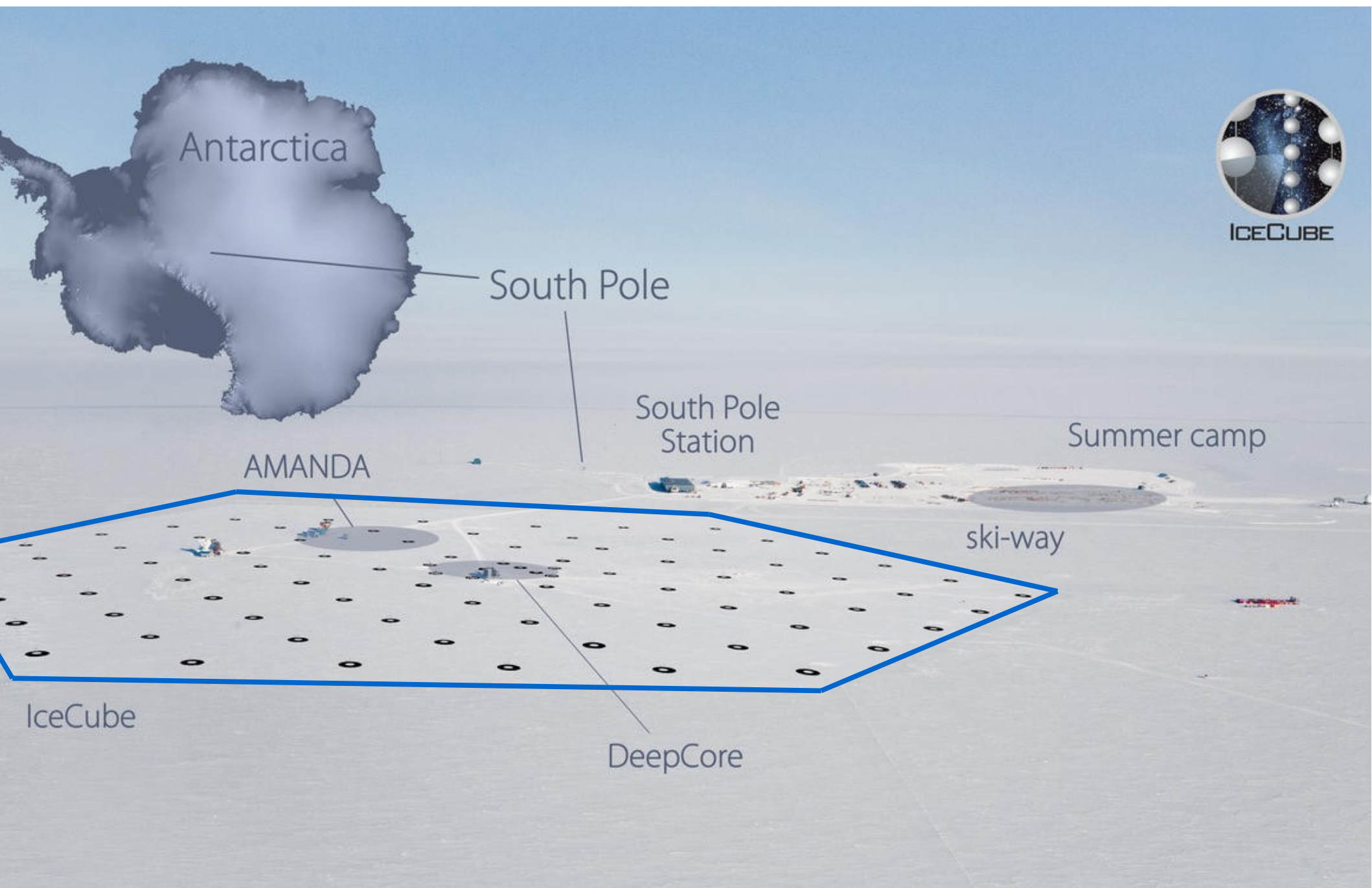


South Pole Station



IceCube Laboratory





Antarctica

South Pole

South Pole
Station

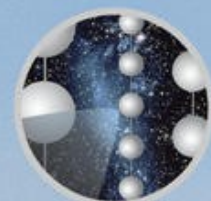
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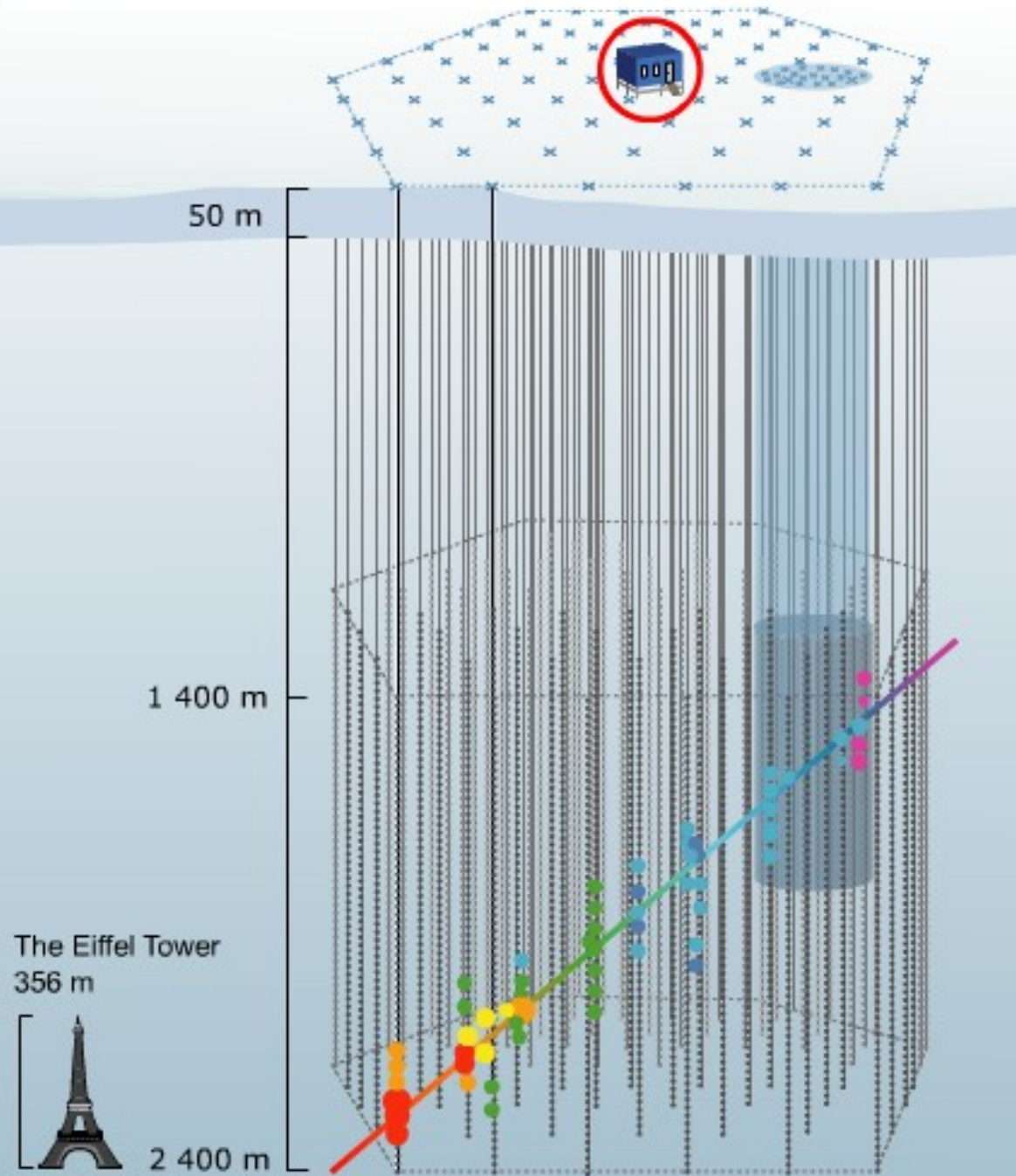
IceCube

DeepCore



ICECUBE

IceCube – a neutrino detector

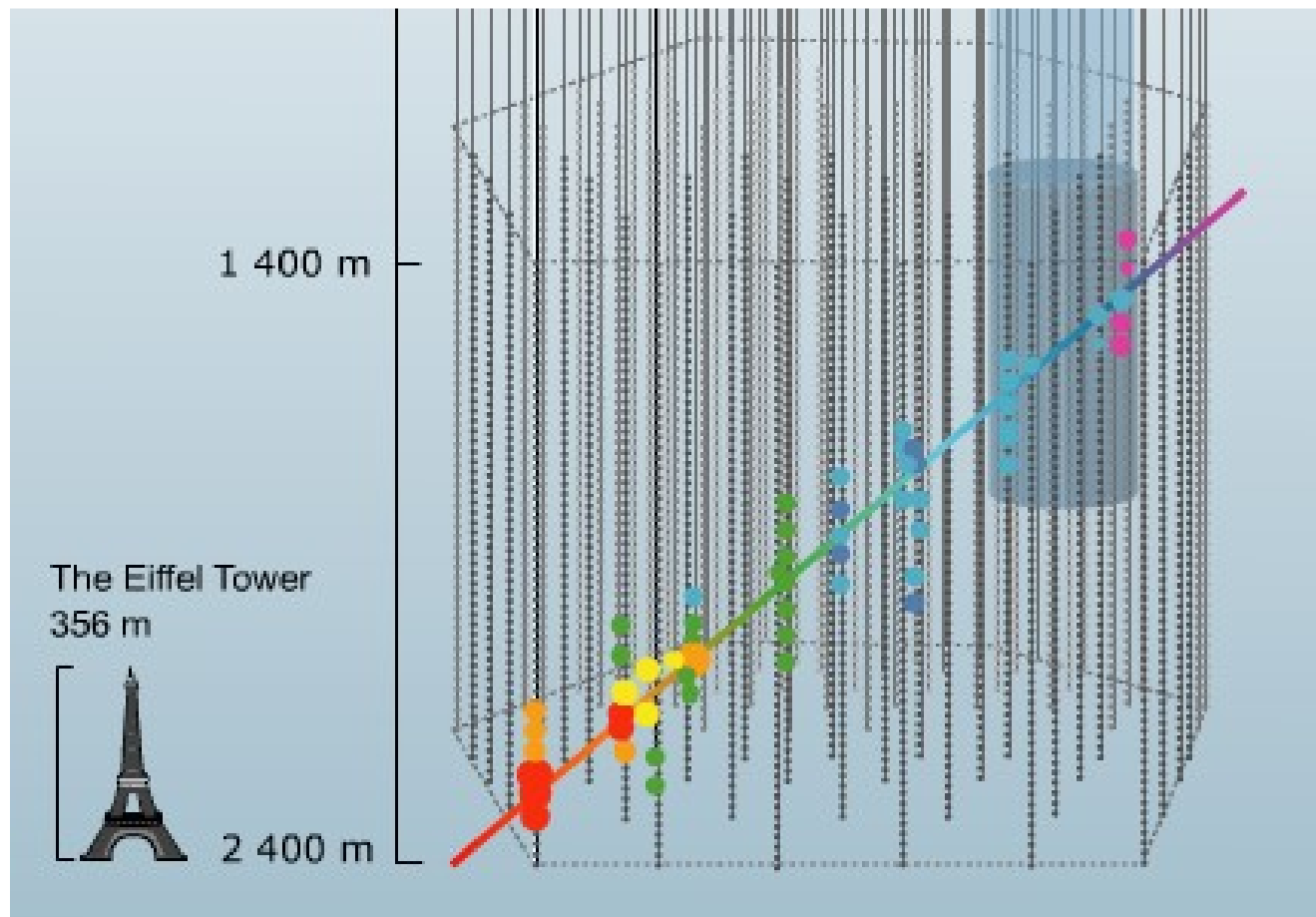


DOM

- Digital Optical Module
- tot. 5160 in full detector
- PMT tubes registering *photons*
- 2.6 million photons/s detected (“hits”) in full detector

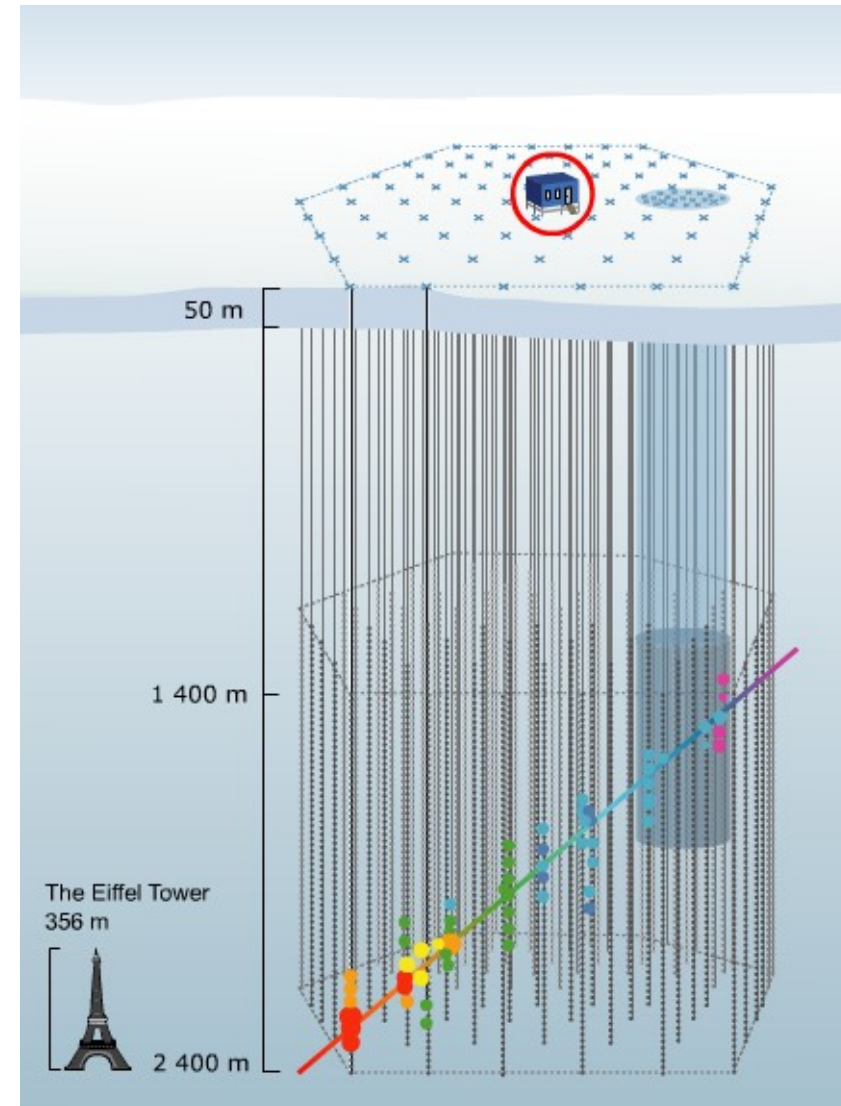
Neutrino \rightarrow muon \rightarrow photon hits along a straight line

(noise hits omitted from picture)



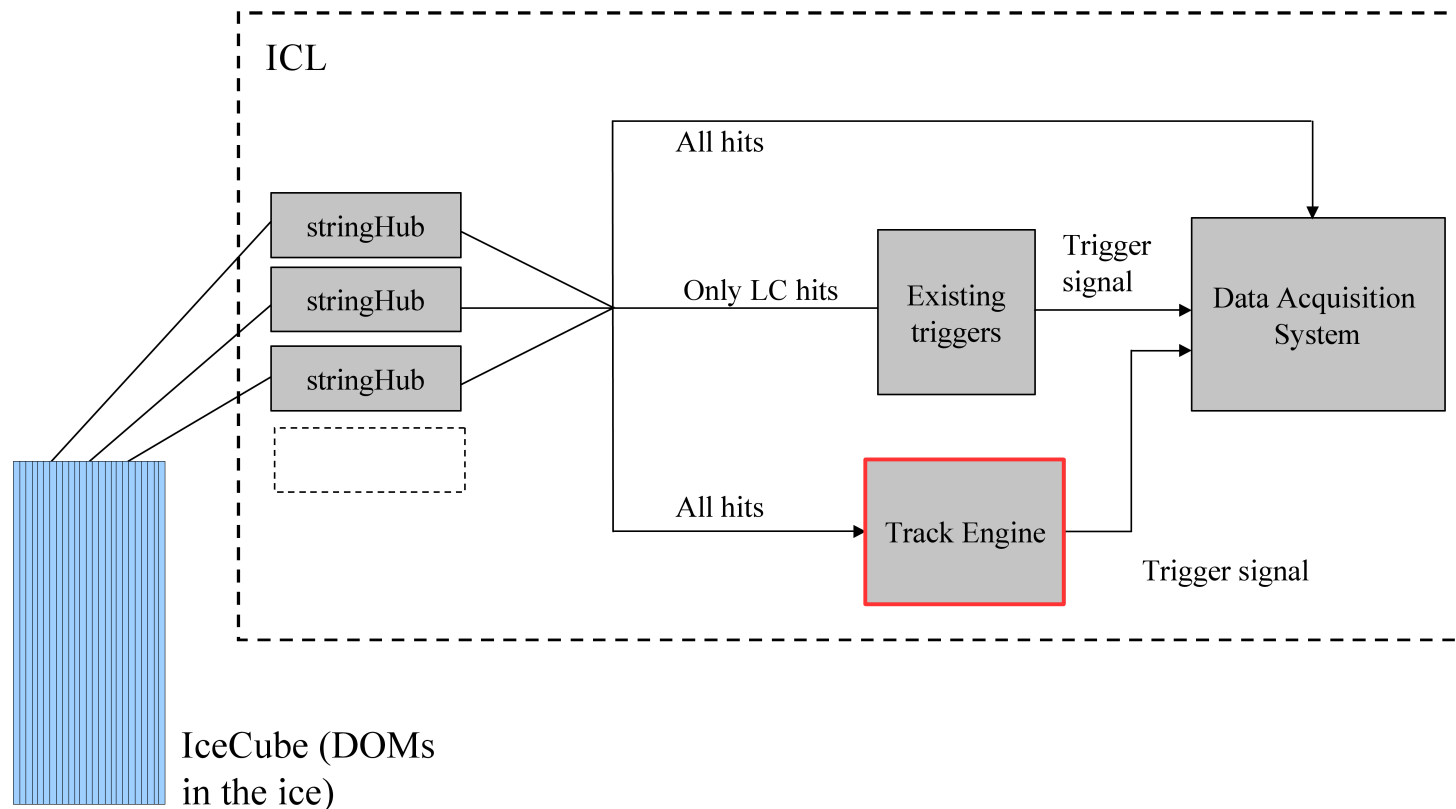
Track Engine – an additional *trigger*

- A *trigger*: select a subset of the data for further processing
- The *Track Engine*: enhanced triggering sensitivity for *low-energy neutrinos*
- Neutrino-induced photons embedded in *noise background*
- Low-energy neutrino \rightarrow fewer photons \rightarrow lower signal/noise ratio

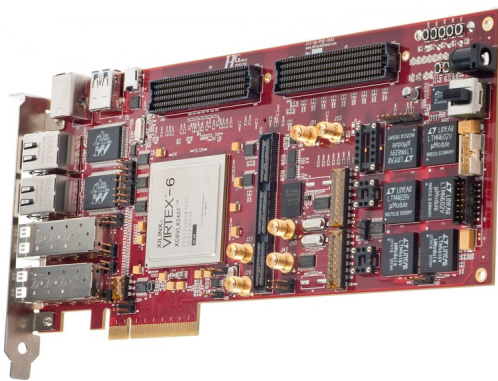
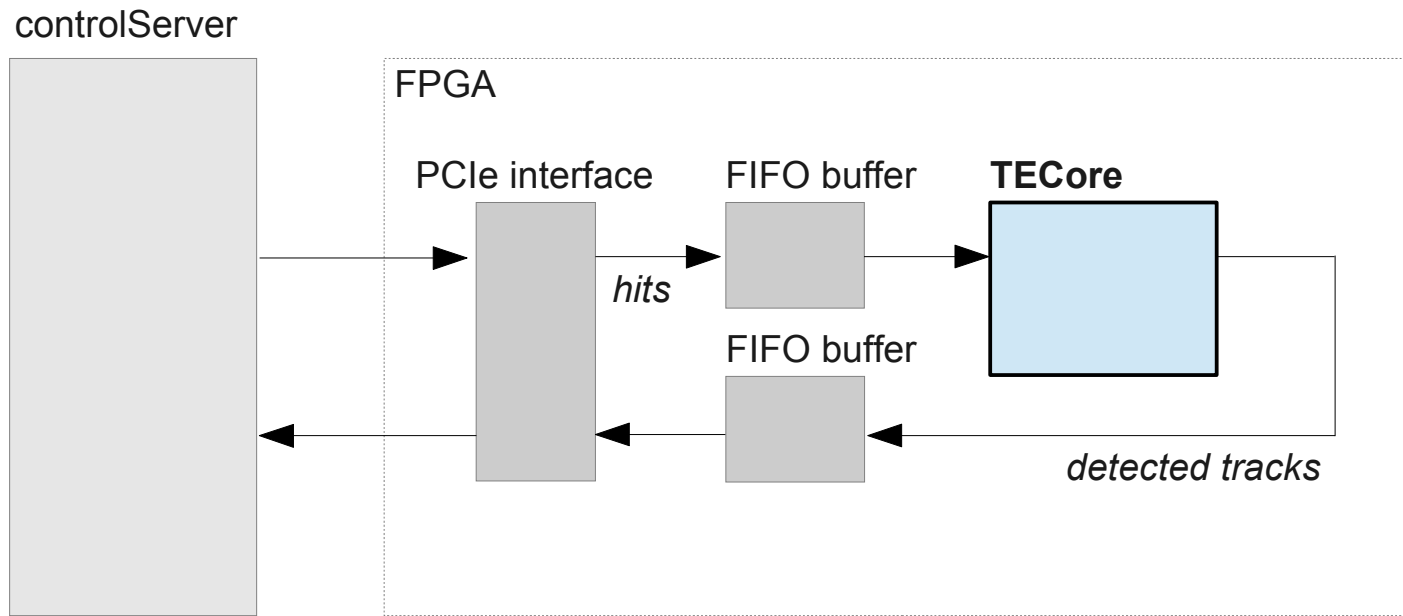


Track Engine (cont.)

- Track Engine, compared with other triggers...:
 - processes *all* hits
 - trigger method based on geometry of the hits



The full Track Engine system



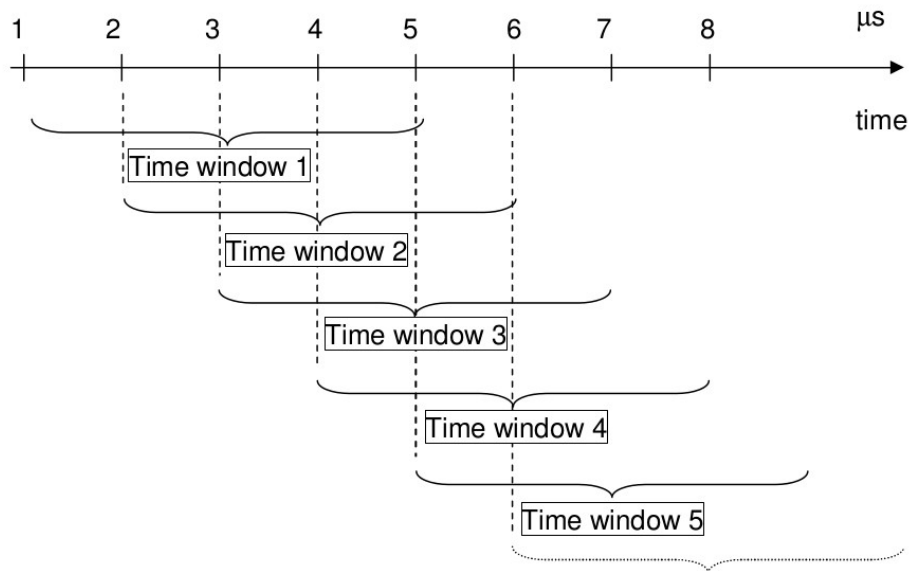
Board: HighTechGlobal HTG-V6-PCIe
FPGA: Xilinx Virtex-6 LX240T -2
Interface: x8 Gen2 PCIe



Host computer (controlServer):
Dell R710 rack server

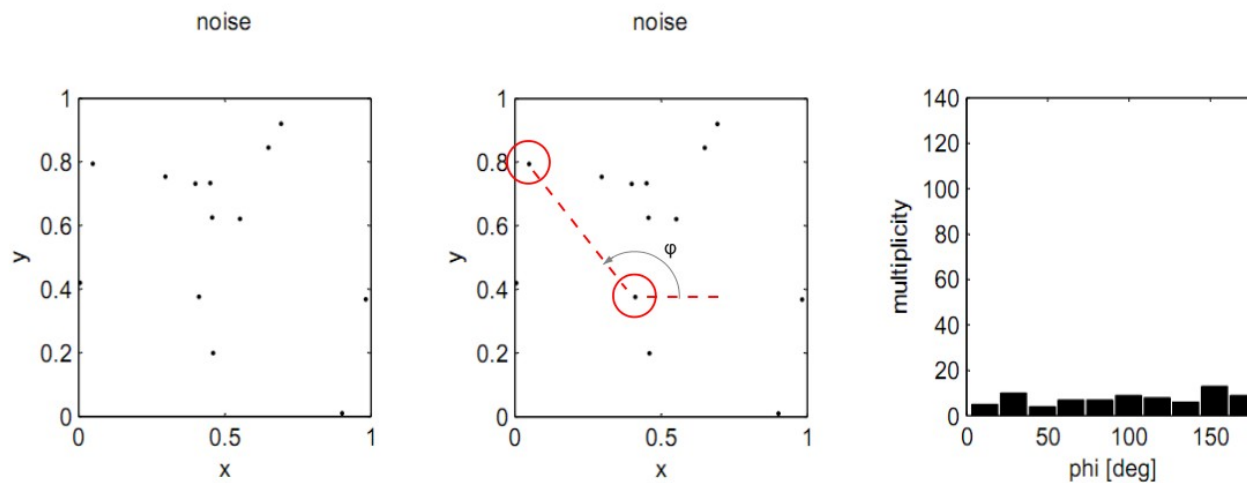
Track Engine Algorithm

- Divide hit stream into overlapping time windows
- Apply the Track Engine algorithm to all hits of each time window
- Time window width = 5 μs , slide 1 μs at a time



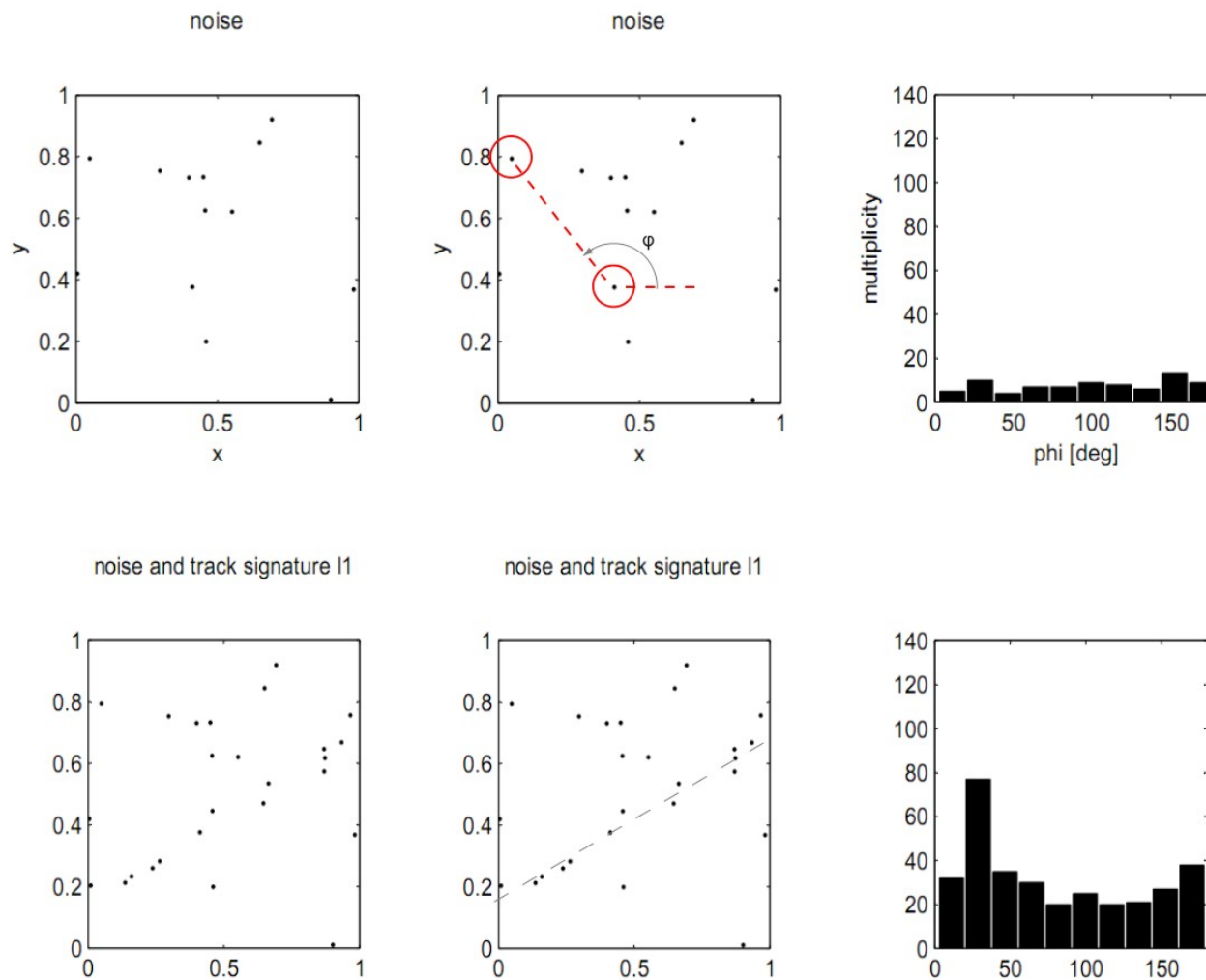
Track Engine Algorithm

- a 2-dimensional example



Track Engine Algorithm

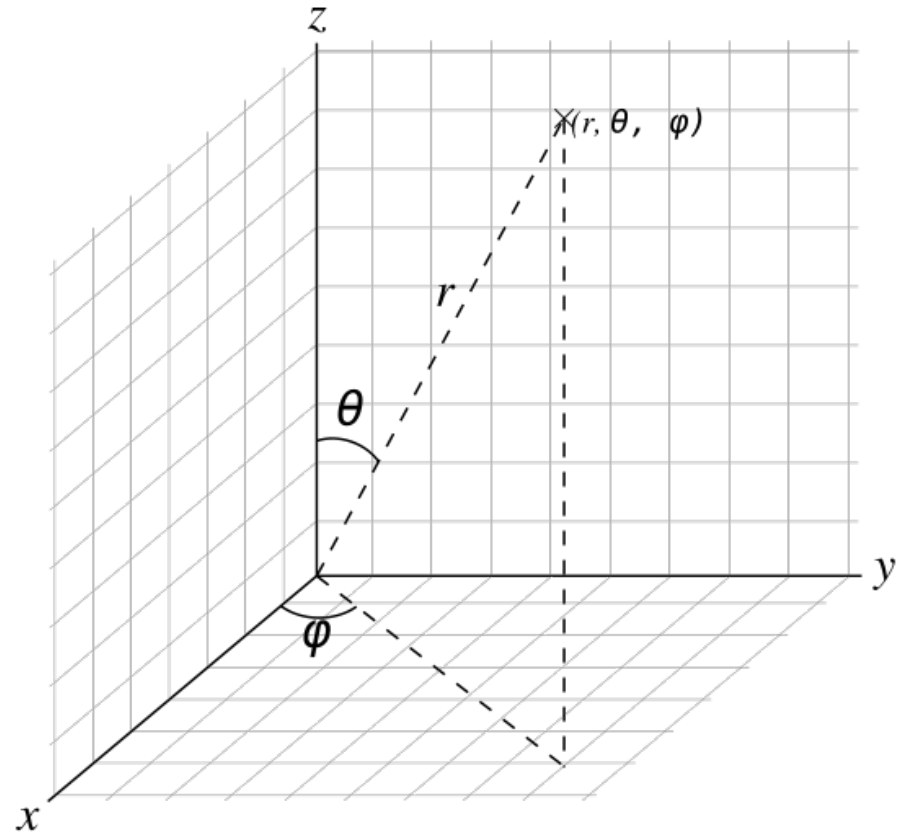
- a 2-dimensional example



Track Engine Algorithm

- for the 3-dimensional detector

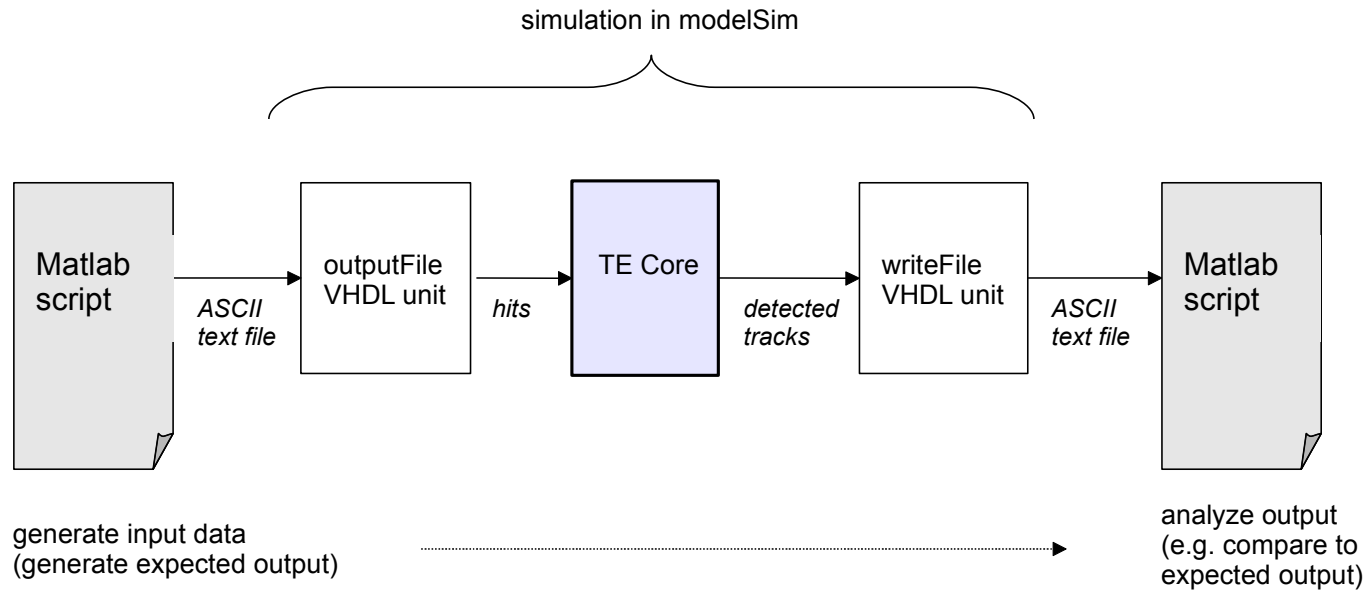
- Two angles, θ and φ of a spherical coordinate system, needed to identify a direction between two hits



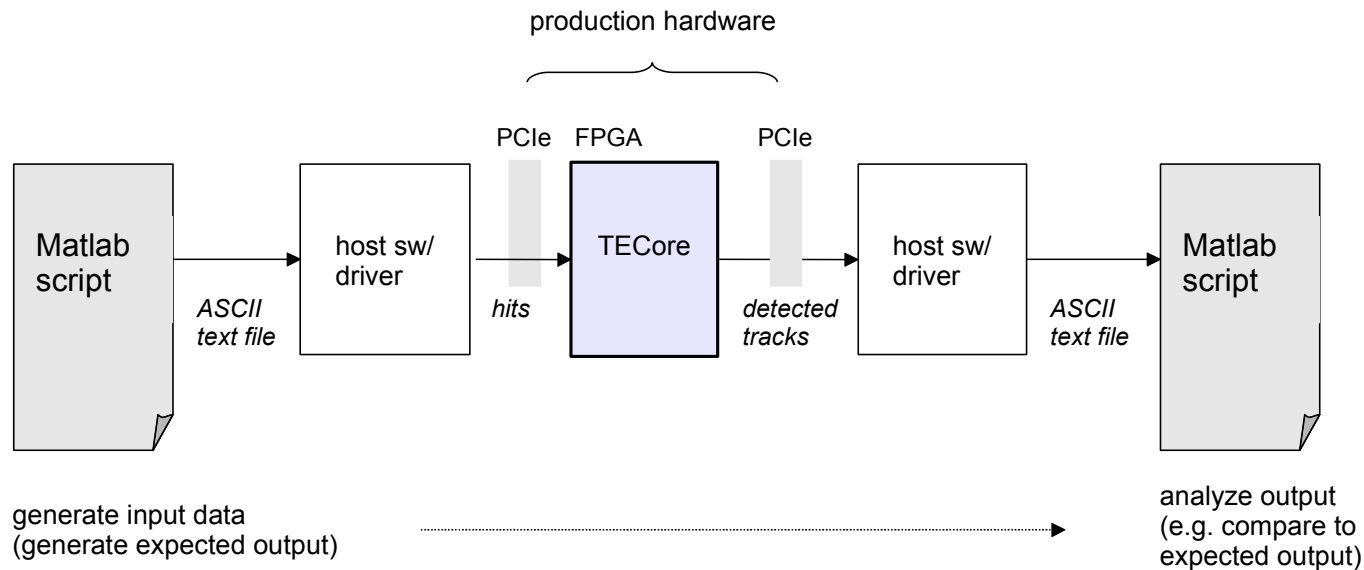
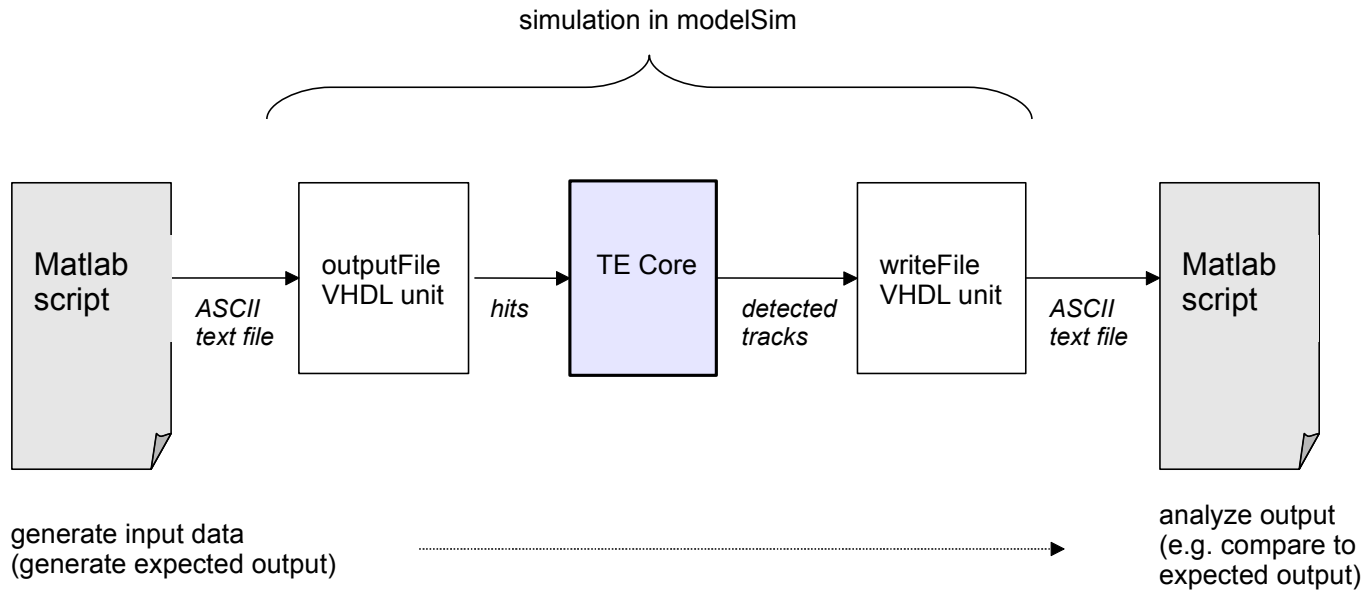
The FPGA implementation

- The algorithm is, in principle, implemented as one long processing data path, without intermediate buffers
 - length: approx. 1500 clock cycles
 - → superior computing performance
- Only integer (as opposed to floating-point) representation used
 - advantage: reduces hardware resources, improves timing and hence performance
 - disadvantage: more complex to develop

Test environment (self-developed)



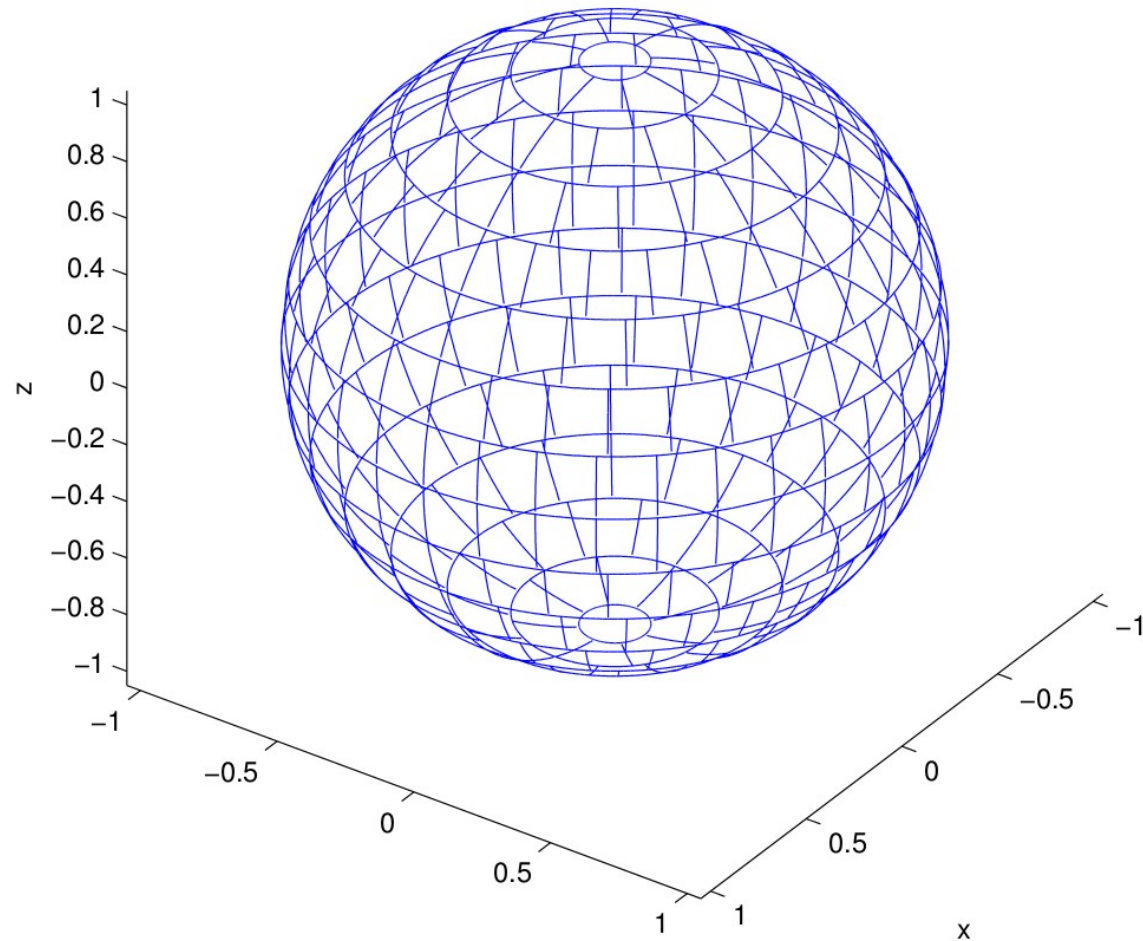
Test environment (self-developed)

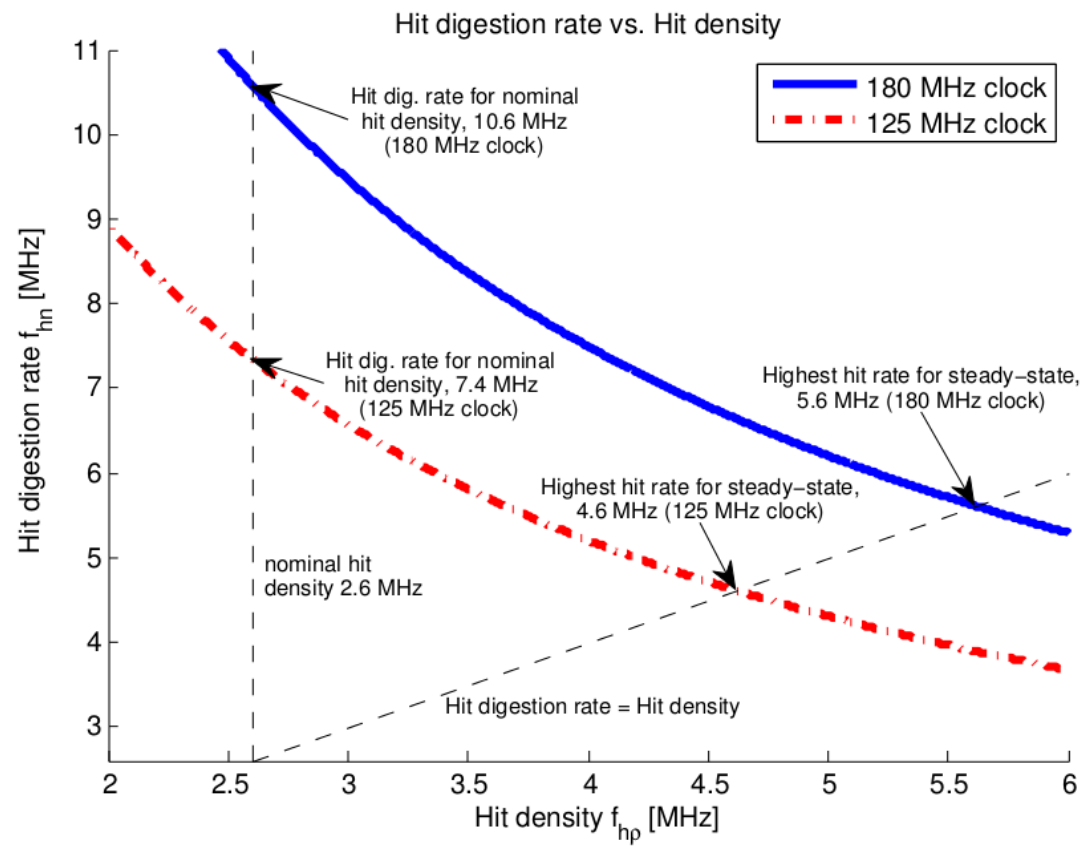


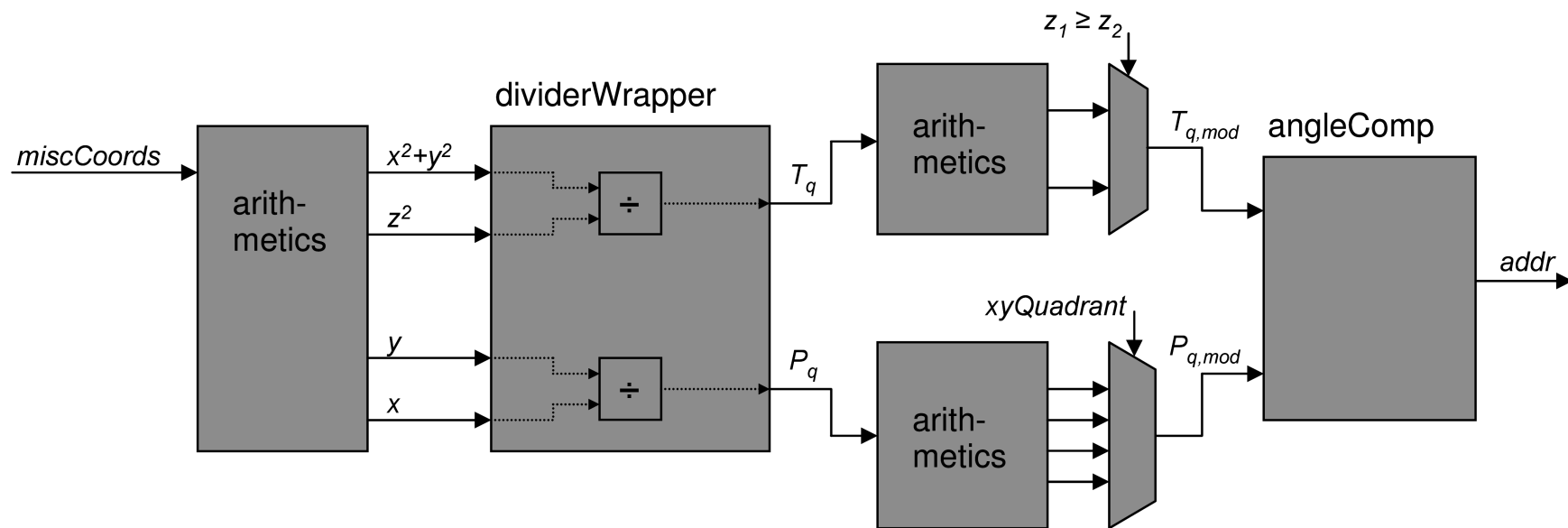
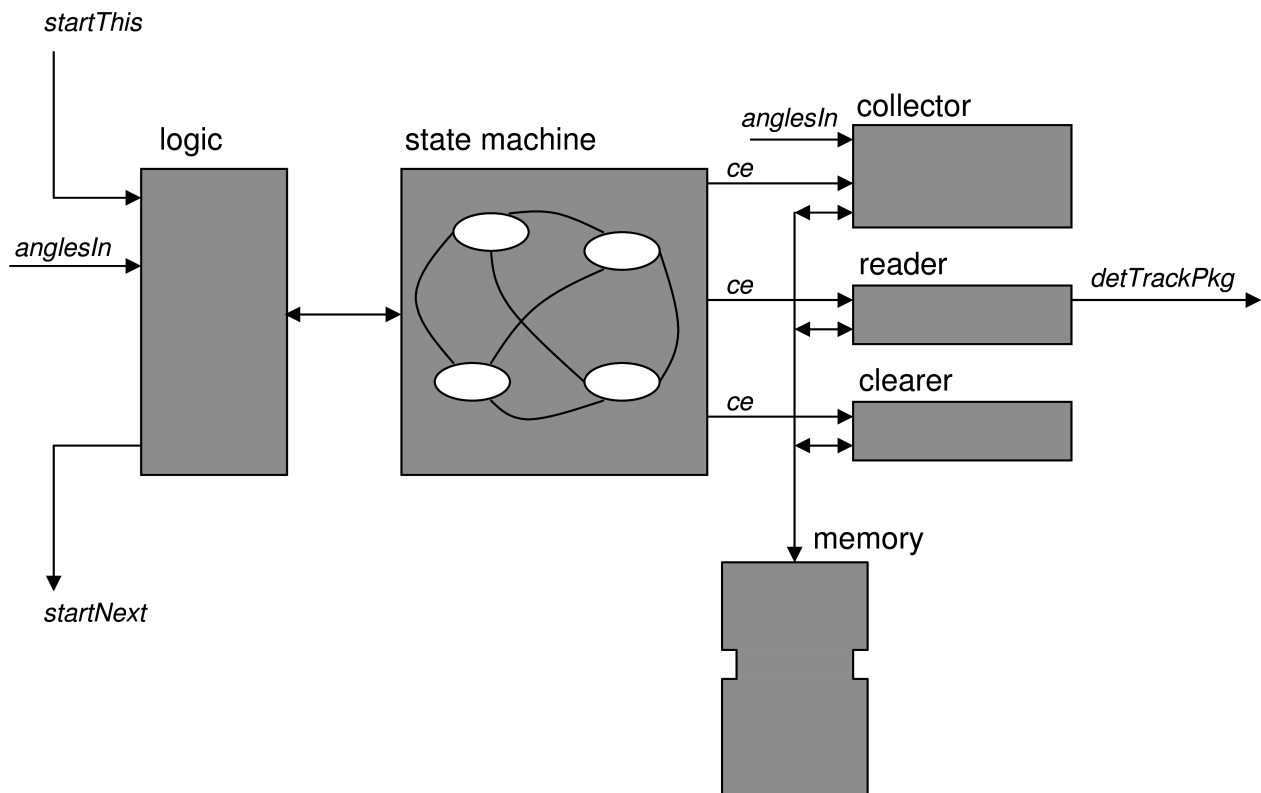


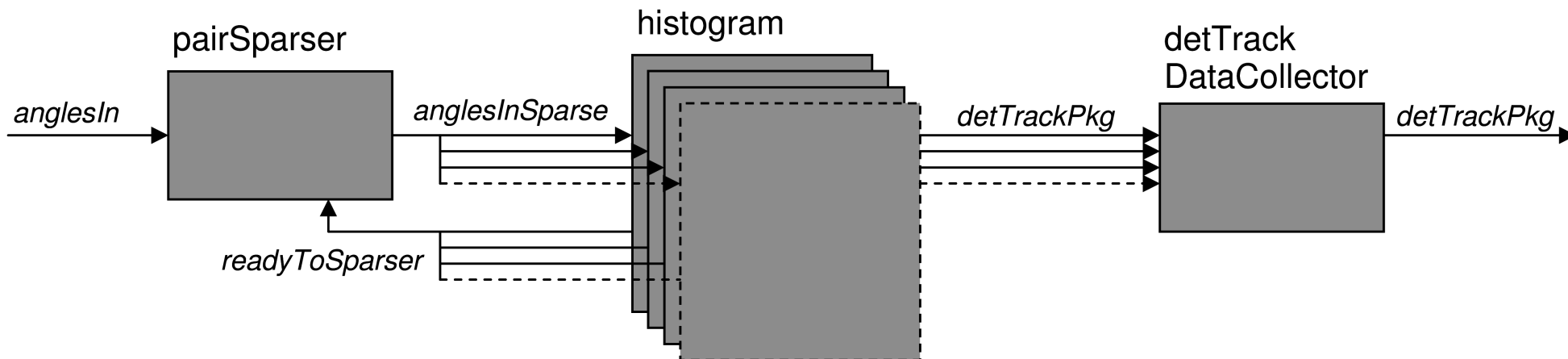
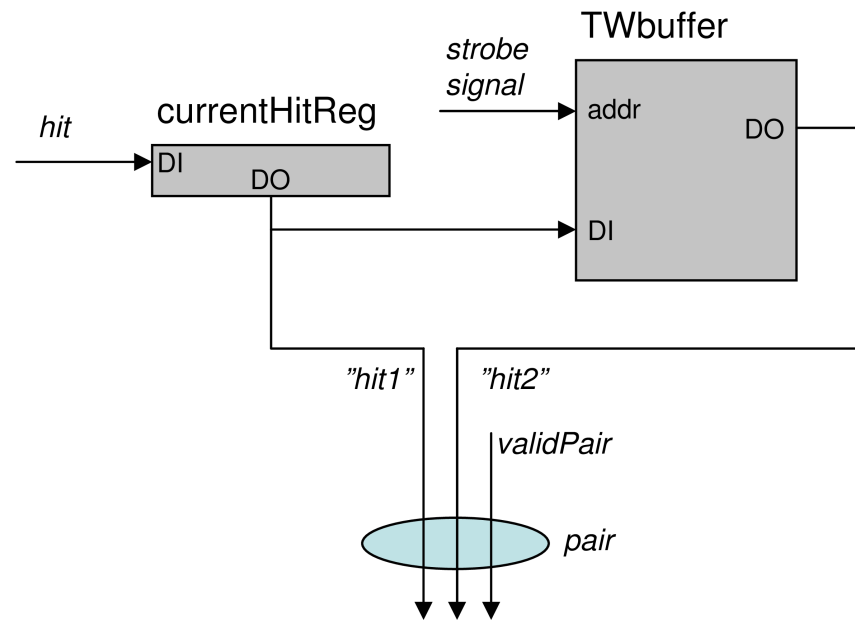
Backup slides

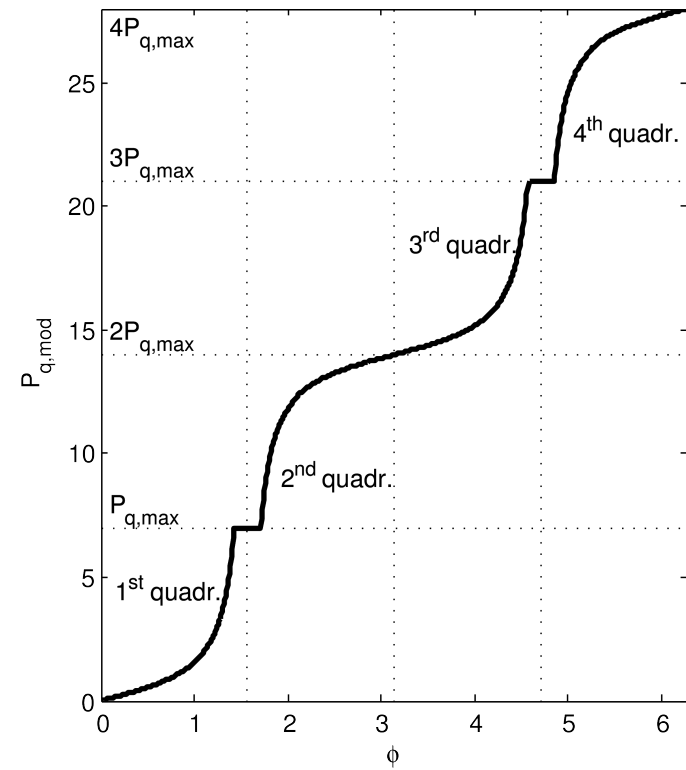
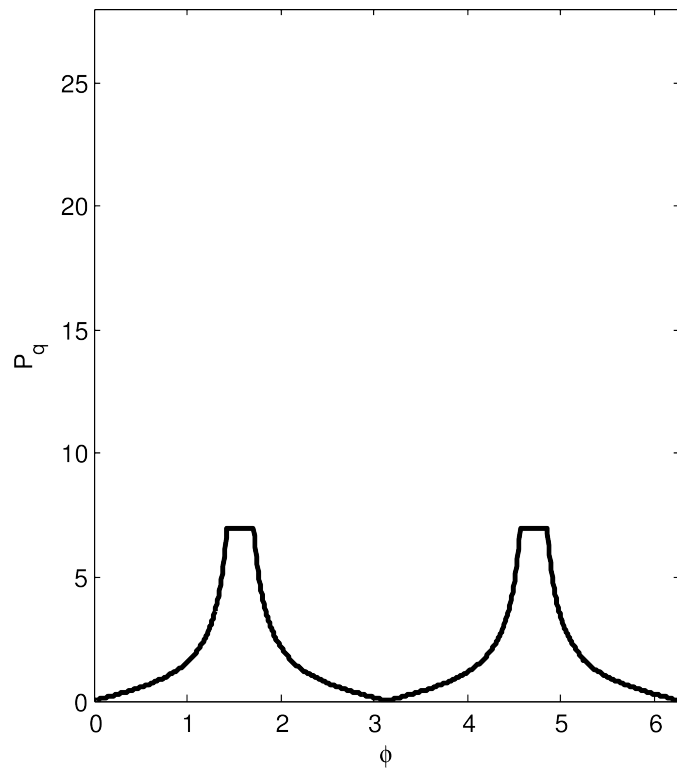
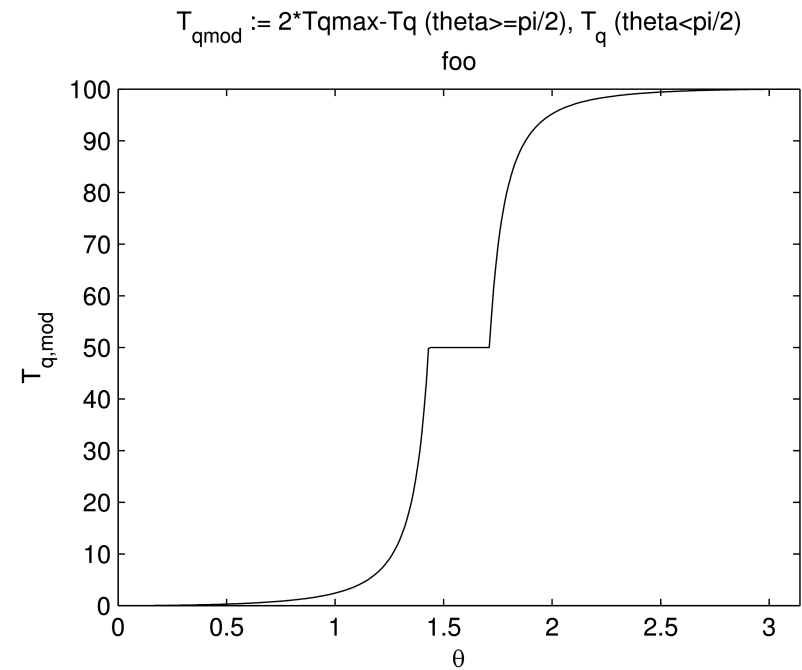
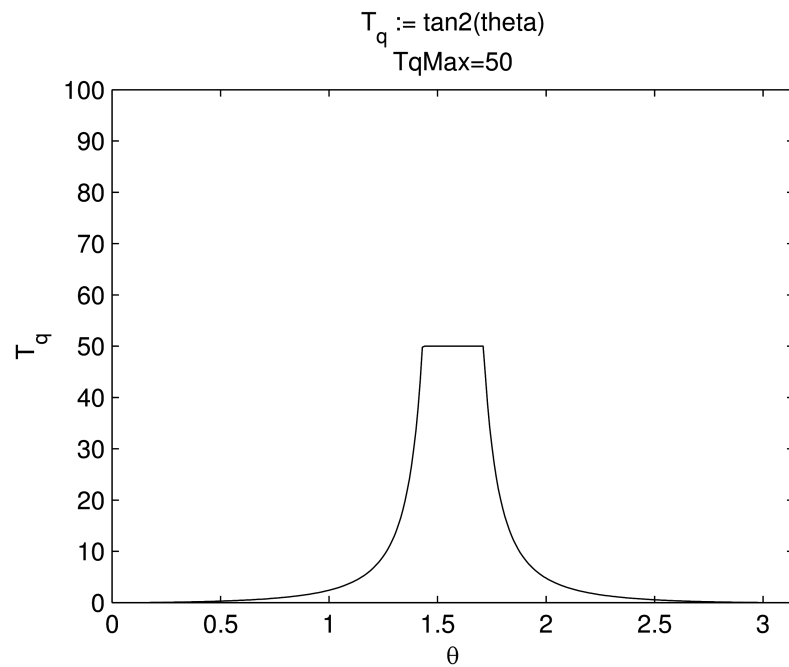
- Histogram bins
 - \rightarrow regions on the unit sphere, defined as θ and φ limits

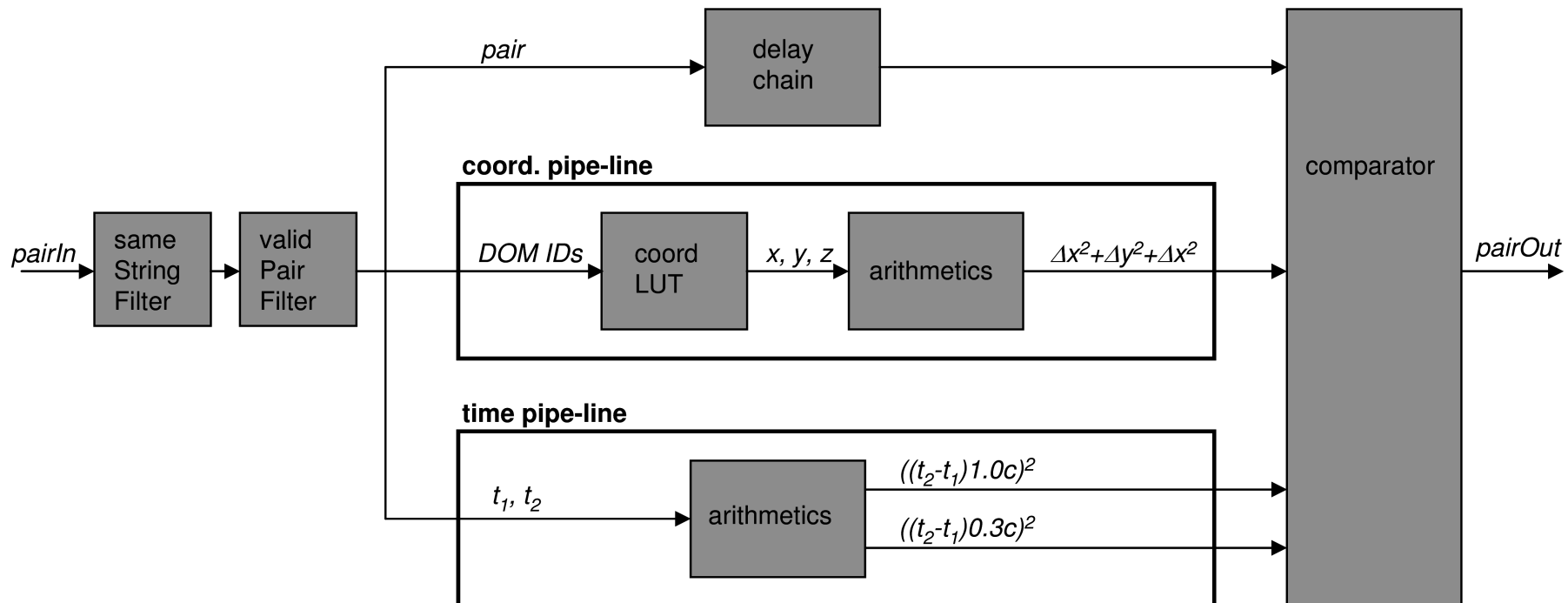












Neutrinos detected by Cherenkov radiation

