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Abstract: Development of a 10G Ethernet UDT Server in FPGA

This presentation describes development of a 10G Ethernet UDT server on a Virtex6 FPGA for a high-speed, high-reliability data recording application. We will look at architecture choices and selection of protocol, architecture for processor and data offload mechanism in FPGA. Lower layers from SFP+ wire to PHY chip and XAUI, XGMII require use of Xilinx Multi Gigabit Transceivers at relatively high clock rates. The protocols Ethernet, ARP, ICMP, IP, UDP and their implementation in FPGA are all a requirement for an efficient and high-performance UDT server implementation. We will see how these layers are handled by hardware and software functions, and look at the verification strategy, simulation, test vectors and other tools such as Wireshark.

The presentation will also cover figures for FPGA resource usage, data transfer rate performance, latency and reliability. Extensive and continuous use over long time demonstrates that FPGAs today are capable of sustained high speed data transfer, using protocols that ensure zero errors using standard off the shelf hardware. The presentation will show how high performance Ethernet connectivity can be quickly and easily embedded through the use of standardized interfaces, widely used tools and test harnesses, which greatly shorten integration time and reduces development effort.