Title: Achieving the right FPGA design quality – Could reviews save the day?
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1. UVVM: Universal VHDL Verification Methodology ("UVM for VHDL")

Most FPGAs and modules have two or more interfaces that need to operate simultaneously, and lots of corner cases arise from the access to these interfaces at more or less random times.
Even a simple module like a UART has lots of corner cases - due for instance to the possibility of CPU reads of the RX-register coming at random times with respect to data actually entering the RX register/FIFO/buffer from the RX interface. To verify that all these corner cases are OK requires simultaneous stimuli (and monitoring) of all interfaces and the ability to skew these accesses with respect to each other. In most TBs this is handled in a very unstructured manner.
Bitvis is now implementing UVVM, and as a first step we handle the most important functionality and the critical infrastructure for this. UVVM provides a simple, structured and reusable approach to this problem. UVVM also allows random stimuli in a controlled manner. Like Bitvis Utility Library anyone can implement such a system, but it requires experience, structure and focus on simplicity. This presentation explains the system and how this significantly improves verification efficiency and quality. It also explains how to build such a system.
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2. FPGA Best Practices - A pragmatic approach to faster and better development

ALL designers and project teams have an improvement potential on quality, efficiency, and making modifiable and well-structured design.
Most do in fact have a huge improvement potential. 'FPGA Development Best Practices' is a two-day course that addresses this potential.
It is a unique course with its pragmatic approach to better structuring, better coding and avoiding the pitfalls and also addressing the worst time wasters and quality risks like clock domain crossing.
The course has been held in Sweden, Denmark and Norway several times - always with a very good feedback.
The course will now be held in Stockholm in October/November 2014 (TBD).
Some general information about the course can be found on our web site.
This presentation will show more details on what this course will cover
- as a teaser to make you understand that this course is relevant for all FPGA designers.